

Part Number

Customer

Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	150.00 +/- 0.20 mm	
	2.0	Primary Flat Orientation	{110} +/- 1.0 degree	Wafer Vendor
	3.0	Primary Flat Length	57.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Length	NONE	Wafer Vendor
	5.0	Overall Thickness	400.00 +/- 5.00 µm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<3.00µm	Guaranteed by Process
	7.0	Bow	<60.00µm	ADE to ASTM F534, 20%
	8.0	Warp	<60.00µm	ADE to ASTM F657, 20%
	9.0	Edge Chips	None	Bright Light, 100% (note 2)
	10.0	Edge Exclusion	5mm	
	11.0	Front Surface Quality	Polished. No frontside scratches. No orange peel, edge chips or other surface defects.	Bright Light, 100% (note 2)
	12.0	Backsurface condition	Polished with light handling marks	Bright Light, 100% (note2)
	13.0	Field Oxidation	22,000.00 +/- 1,100.00 A	Nanospec centre point, 4%
	14.0	Lasermarking	Laser Scribe on backside. IceMOS Standard format: YYMM-XXXXXX	
	15.0	Backside Laser Marking Location	Left Hand Side of Wafer Flat, 2.2mm from wafer edge.	
	16.0	Edge Rounding	Edge profile to suit 400um DSP thickness.	IceMOS Internal - Edge profile to suit 400um DSP wafer.
HandleSilicon	17.0	Handle Silicon Raw Material	Prime Silicon	
	18.0	Handle Growth Method	CZ, MCZ or FZ	Wafer Vendor
	19.0	Handle Orientation	{100} +/- 0.5 degree	Wafer Vendor
	20.0	Handle Thickness	400.00 +/- 5.00 µm	ADE, 100%
	21.0	Handle Doping Type	P	Wafer Vendor
	22.0	Handle Dopant	Boron	Wafer Vendor
	23.0	Handle Resistivity	1 ~ 10 Ohmcm	Wafer Vendor
	24.0	Handle Oxygen Concentration	<15ppma ASTM-83; new	Wafer vendor
	25.0	Backside Finish	Polished, with lasermarking. Light handling scrtaches.	Guaranteed by process
	26.0	Surface Haze	none	Bright Light, 100% (note 2)

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Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	

Explanatory Notes	1. Microscope inspection performed using microscope scan as below. 5x objective.		
	2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.		
	3. 9 point measurement are as shown in the diagram below:		



Additional Information