

IceMOS

Technology



Product Brief

High Voltage

MEMS Super junction MOSFET

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1. Scope:

This **Product Brief** supplies information about IceMOS Technology’s high voltage Superjunction MOSFET products containing electrical characteristics and proposed application circuits. The product brief is intended for Engineers involved in the design of circuits for power module products.

2. Electrical Characteristics

2.1 Maximum ratings

Example of ICE20N170 ($T_j=25^\circ\text{C}$)

Maximum ratings , at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Condition	Value	Unit
Continuous drain current	I_D	$T_c=25^\circ\text{C}$ $T_c=100^\circ\text{C}$	20 11	A
Pulsed drain current	$I_{D, \text{pulse}}$	$T_c=25^\circ\text{C}$	62	A
Avalanche Energy, single pulse $E_{AS}=1/2*L*I^2(V_{BRDSS}/(V_{BRDSS}-V_{DSS}))$	E_{AS}	$I_D=10\text{A}$	520	mJ
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=480\text{V}$, $I_D=5\text{A}$, $T_j=125^\circ\text{C}$	50.0	V/ns
Avalanche current, repetitive	I_{AR}	limited by T_{jmax}	10	A
Gate source voltage	V_{GS}	Static	± 20	V
		AC ($f > 1\text{Hz}$),	± 30	
Power dissipation	P_{tot}	$T_c=25^\circ\text{C}$	236	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	$^\circ\text{C}$
Mounting torque ^a		M 3 & 3.5 screws	60	Ncm

^a When mounted on 1inch square 2oz copper clad FR-4

2.1.1 E_{AS} Avalanche Energy

E_{AS} Avalanche Energy is the energy surge when the MOSFET is switched off due to Induced Current flow from Inductance(L) it is illustrated below as a simple equation

$$E=L*di/dt$$

In the test circuit, ON time was adjusted to create Inductance(L) and keep a certain level of current energy. The current was then forced through the Test device at switch off. This test is called a UIS Test (Unclamped Inductive Switching) providing the amount of energy the device can survive by test giving an indication of the device robustness.

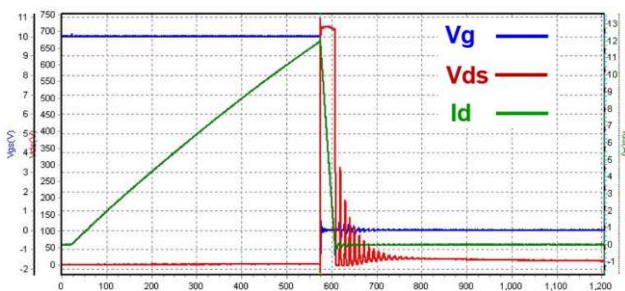


Fig. 1 output wave example of UIS test.

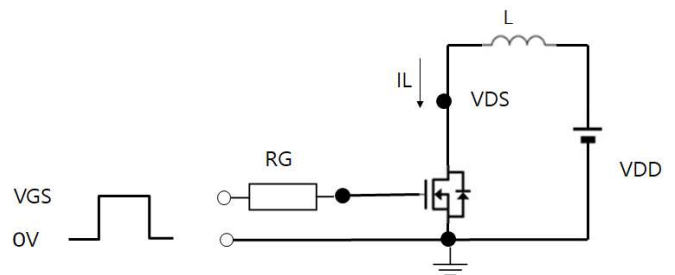


Fig.2 Example of UIS circuit

2.1.2 MOSFET dv/dt ruggedness

The Parasitic npn bipolar transistor in the SJMOSFET is shown in Fig4. When the voltage is changed with dv/dt at Turn off, Current flows through Capacitor C and Resistor R. Since this current creates a Voltage due to the resistance the gate of the parasitic npn bipolar transistor may turn ON and further current may flow which may lead to MOSFET destruction by this phenomenon.

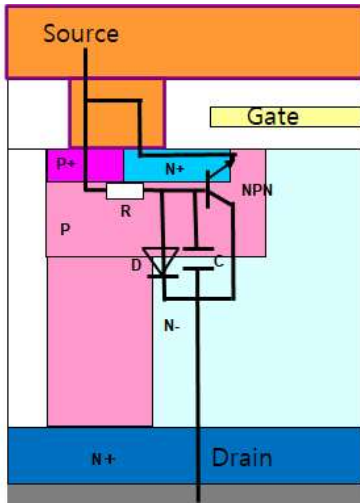


Fig.3 Parasitic npn Transistor

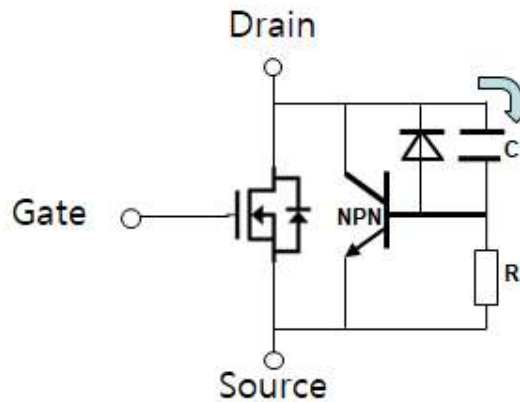


Fig.4 Equivalent Circuit

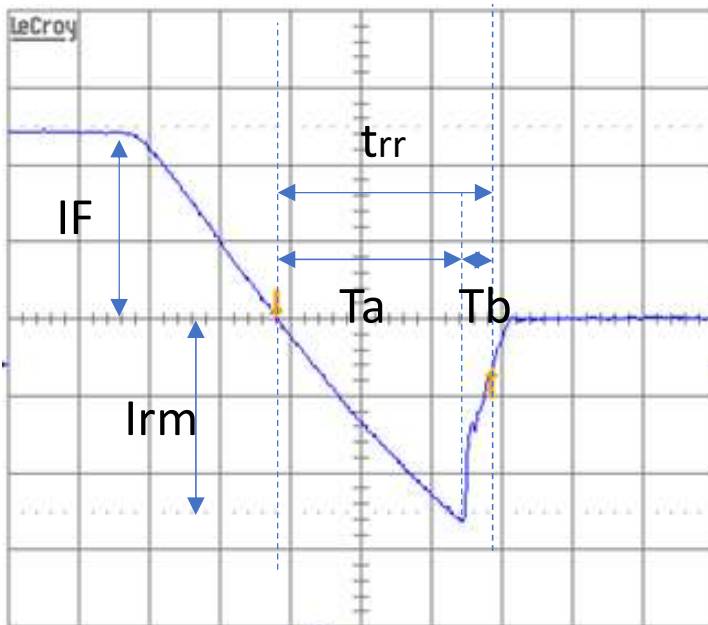


Fig.5 Trr waveform at Reverse recovery

Time Ratio T_b/T_a could be soft recovery index.

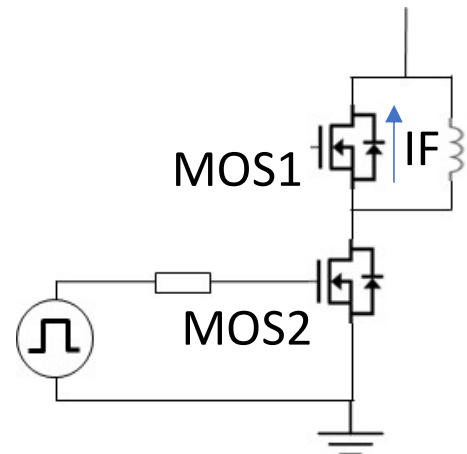
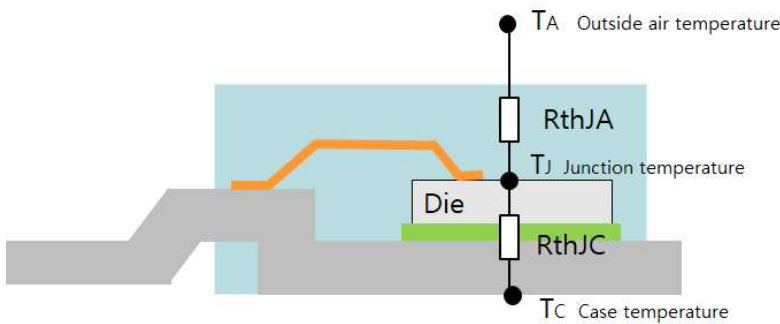


Fig.6 Switching circuit example. When the Current flows through MOS2 and is then turned off, IF current flows through MOS1. When MOS2 is turned on again, this current flows through MOS2, the voltage of the body diode of MOS1 rises showing reverse recovery operation, and current waveform is shown by this change of dv/dt in Fig5.

2.2 Thermal Characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Thermal characteristics						
Thermal resistance, junction-case ^a	R_{thJC}		-	-	0.53	°C/W
Thermal resistance, junction-ambient ^a	R_{thJA}	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C



$$P_{tot} = I^2 * R_{max} * T_c = (T_J - T_c) / R_{thJC}$$

$$= (150 - 25) / 0.53$$

$$235.8491$$

Fig.7 Definition of each temperature point and how to calculate Power dissipation P_{TOT} . P_{TOT} can be calculated based on R_{thJC} .

2.2.1 Guidelines for soldering

(Refer to Lead free process by JSTD020/JSTD-020)

Method	Solder Temperature	Duration time	Times
Flow/ Reflow	260°C MAX	10 sec MAX	2 times
Soldering iron	380°C MAX	3 sec MAX	1 time

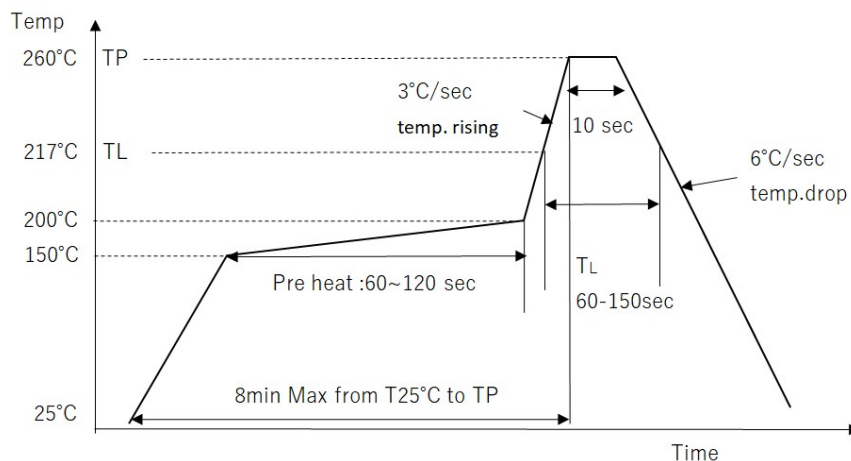


Fig.8 An Example of a Flow Temperature Profile.

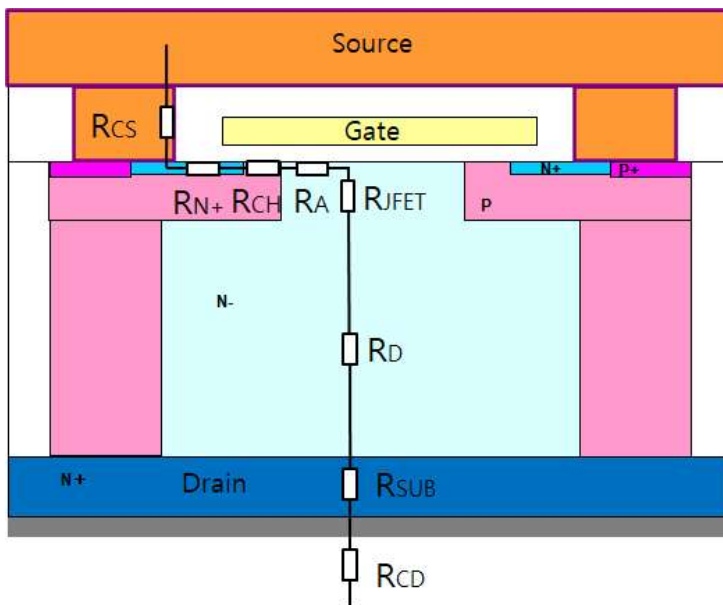
2.3 Static Characteristics (DC characteristics) ($T_j=25^\circ\text{C}$) † :Temperature dependent

Parameter	Symbol	Conditions	Value			unit
			Min	Typ	Max	

Electrical characteristics , at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage † Relationship with P and N Charge balance , $R_{DS(ON)}$	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	600	650	-	V
Gate threshold voltage † Affect switching performance	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current †	I_{DSS}	$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$	-	0.1	1	μA
		$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=150^\circ\text{C}$	-	100	-	
Gate source leakage current	I_{GSS}	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance † Important parameter for on-state power loss	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=10\text{A}, T_j=25^\circ\text{C}$	-	0.17	0.199	Ω
		$V_{GS}=10\text{V}, I_D=10\text{A}, T_j=150^\circ\text{C}$	-	0.49	-	
Gate resistance	R_G	$f=1\text{ MHz}, \text{open drain}$	-	3.8	-	Ω



$R_{DS(ON)}$ is total summary of Below Resistance :

- R_{CS} : Source contact Resistance
- R_{N+} : Source N+ Resistance
- R_{CH} : Channel Resistance
- R_D : Drift Resistance(Main resistance)
- R_{JFET} : JFET Resistance
- R_A : Accumulation Resistance
- R_{SUB} : Substrate resistance
- R_{CD} : Drain Contact Resistance

Fig. 9 The Components of ON Resistance

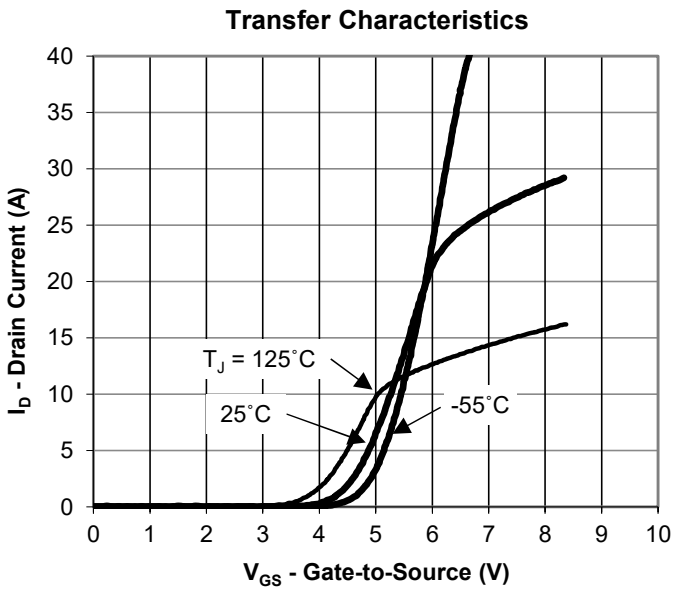


Fig 10 V_{GS} - I_{DS} Characteristic
Voltage beyond $V_{GS(th)}$ can flow a Drain- Source current. Current can be different depending on the Temperature.

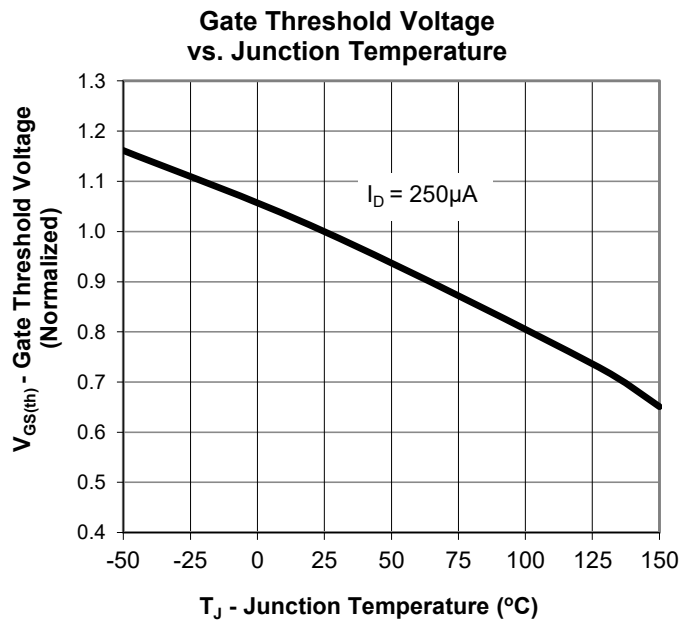


Fig.11 $V_{GS(th)}$ Vs T_J Junction temperature.

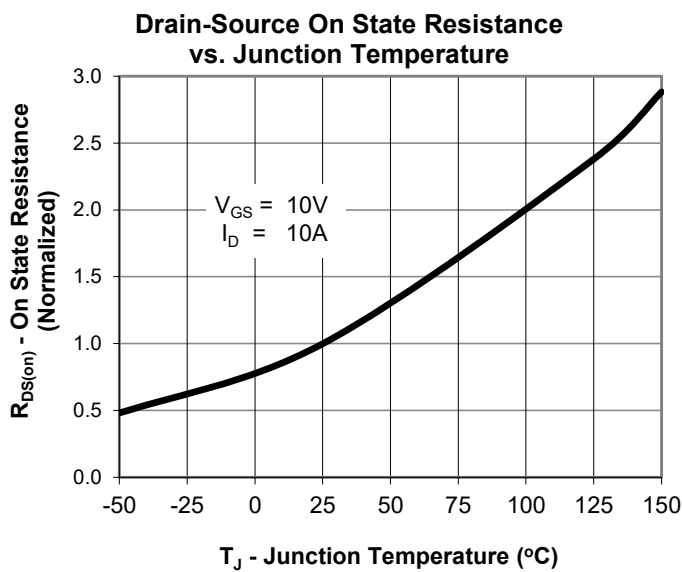


Fig.12 $R_{DS(ON)}$ Vs T_J Junction temperature.

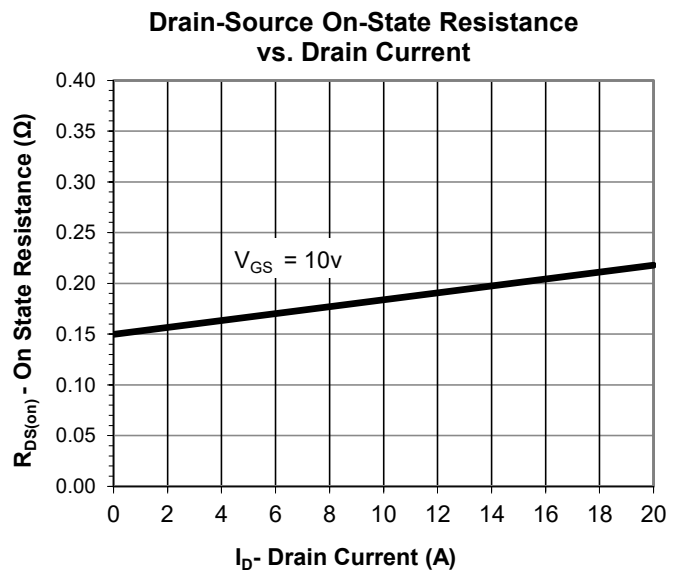


Fig.13 $I_D - R_{DS(ON)}$

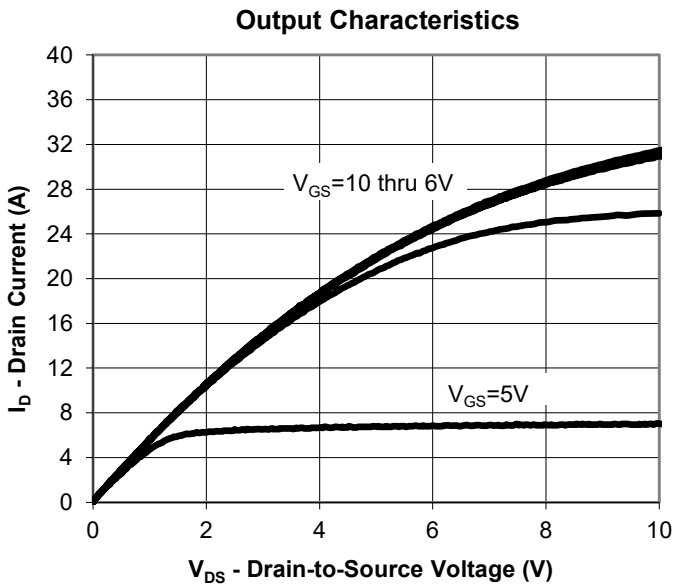


Fig.14: $V_{DS}-I_D$
By raising Gate Voltage over $V_{GS(th)}$, the drain current flows depending on the Drain Voltage.

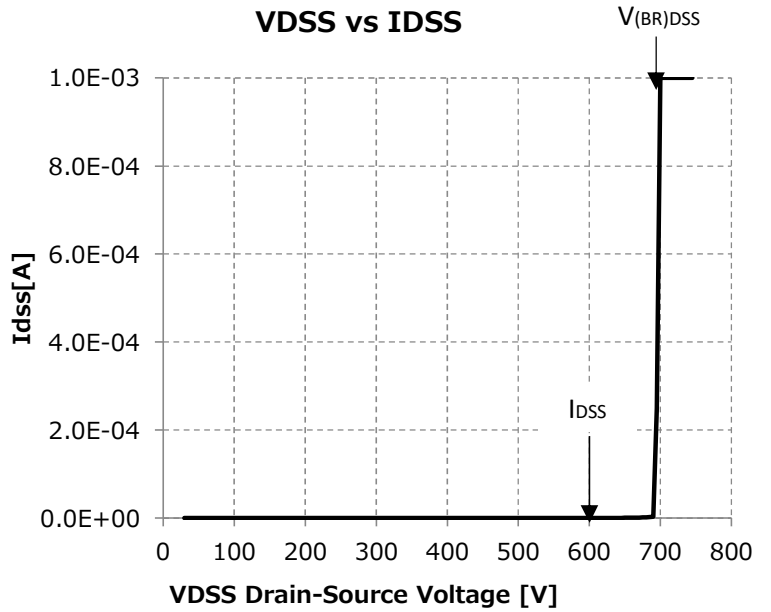


Fig.15: $V_{DSS}-I_{DSS}$
When a voltage is applied between the drain and source when Gate voltage =0V, an Avalanche current begins to flow, and the voltage that reaches the specified current at that time is the breakdown voltage ($V_{(BR)DSS}$)

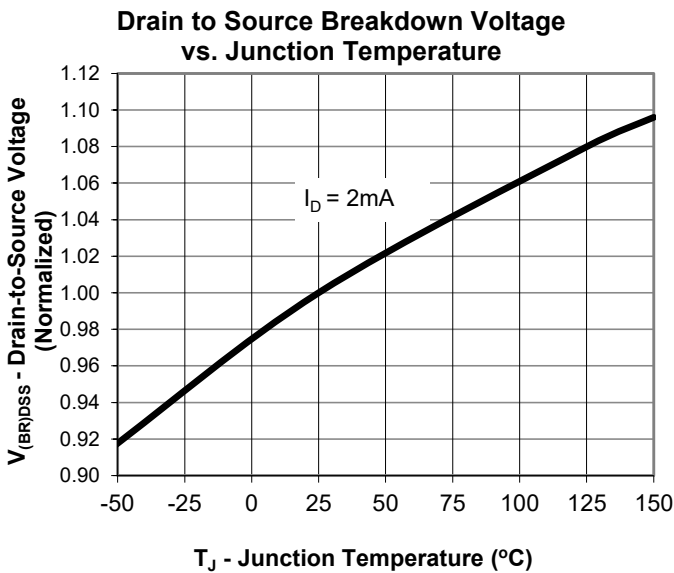


Fig.16 $V_{(BR)DSS}$ Vs T_J Junction temperature.
At 25°C the normalized ratio for $V_{(BR)DSS}$ as V_{DSS} is 1 this subsequently increases with increasing temperature.

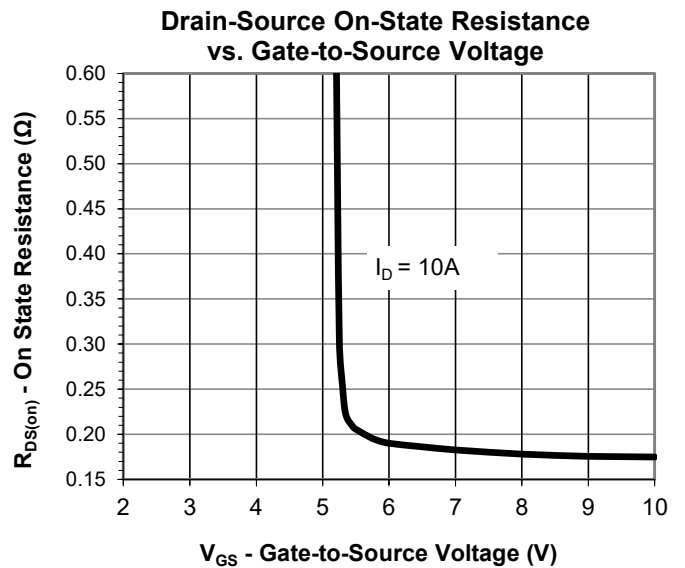


Fig.17 $V_{GS}-R_{DS(ON)}$
The graph shows the required V_{GS} voltage for $I_D=10A$ and the corresponding $R_{DS(ON)}$ value.

2.4 Dynamic characteristics (AC characteristics) ($T_j=25^\circ\text{C}$) ↓ :temperature dependability

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, f=1\text{ MHz}$	$V_{DS}=25\text{ V}$	-	2064	-	pF
Output capacitance	C_{oss}		$V_{DS}=100\text{ V}$	-	87	-	
Reverse transfer capacitance	C_{rss}		$V_{DS}=25\text{ V}$	-	18	-	
Transconductance	g_{fs}	$V_{DS}>2 \cdot I_D \cdot R_{DS}, I_D=10\text{ A}$	-	17	-	S	
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{ V}, V_{GS}=10\text{ V}, I_D=10\text{ A}, R_G=4\Omega$ (External)	-	-	23.2	-	ns
Rise time	t_r		-	-	11.8	-	
Turn-off delay time	$t_{d(off)}$		-	-	92.5	-	
Fall time	t_f		-	-	3.9	-	

Capacitance

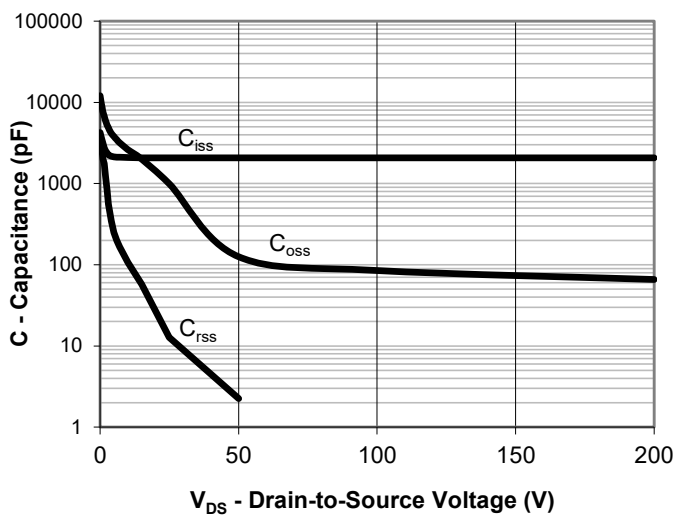


Fig. 18 $C_{iss}, C_{oss}, C_{rss}$ vs V_{DS}

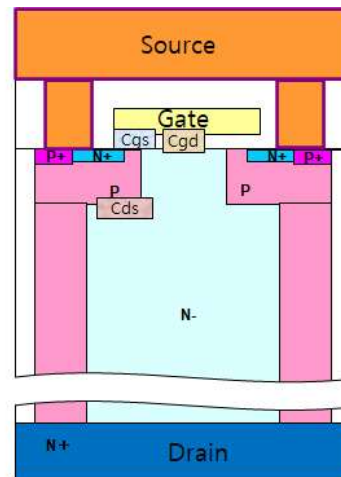


Fig19. Capacitance of the SJMOSFET structure

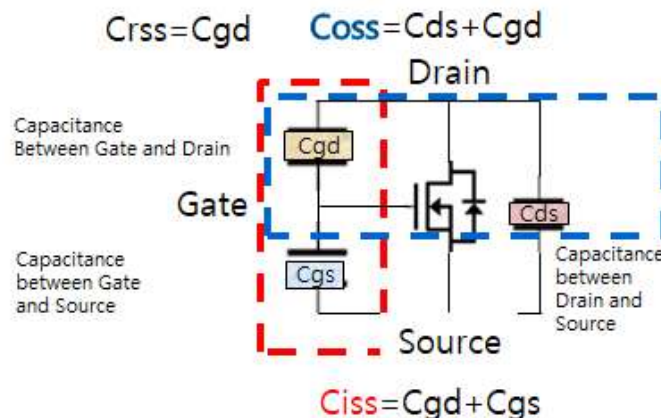
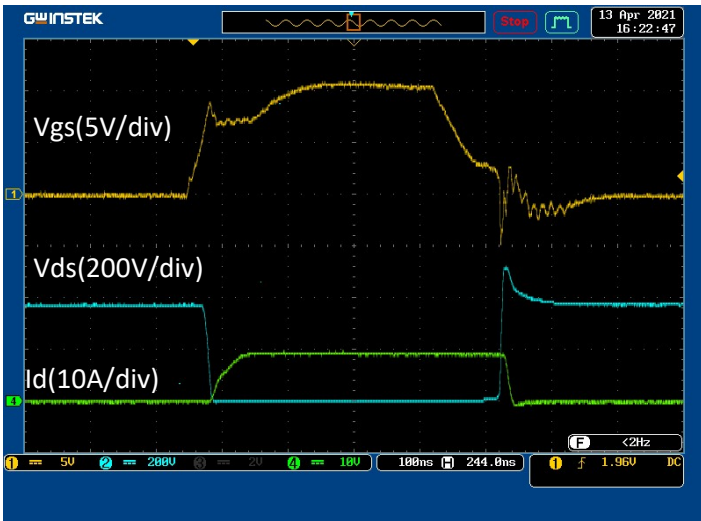


Fig20. Equivalent circuit for capacitance with labelled parameters: $C_{iss}, C_{oss}, C_{rss}$

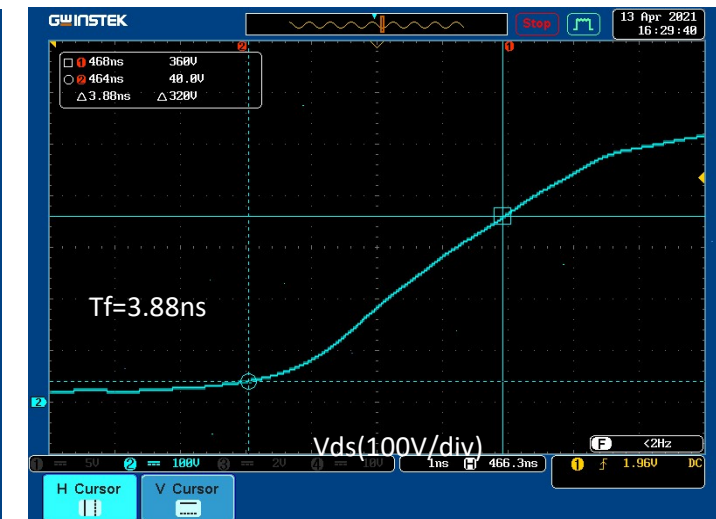
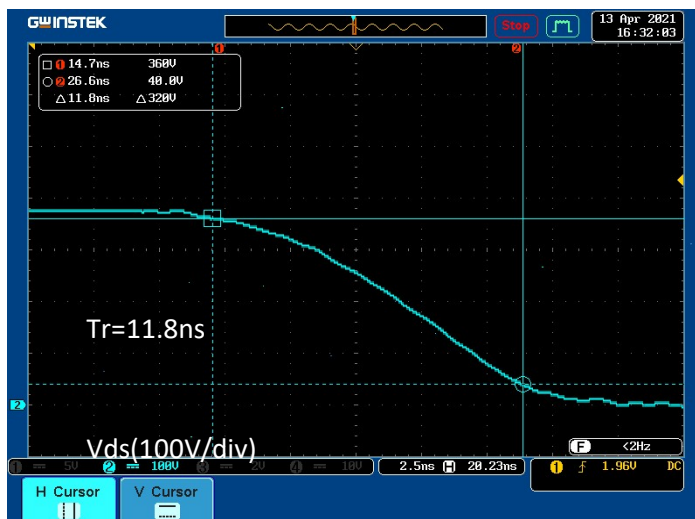
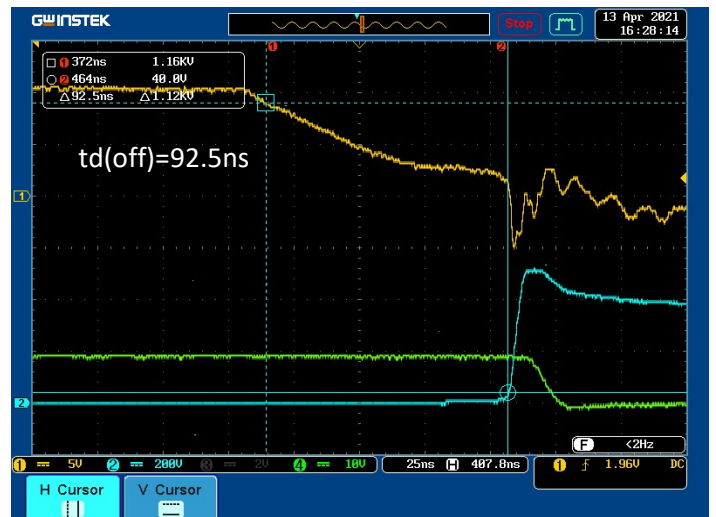
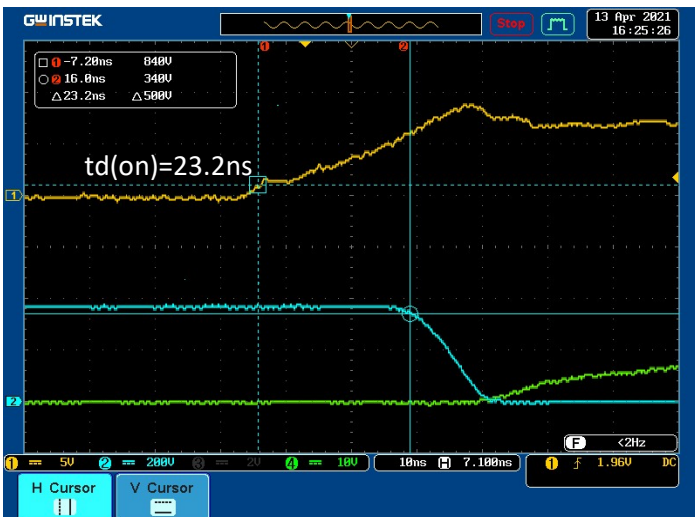
Fig21. Switching waveform for the case of ICE20N170 at Id 10A.



Td (on) (ns)	tr (ns)	Td (off) (ns)	Tf (ns)	Condition
23.0	11.5	82.2	5.5	VDS=380V VGS=10V ID=20A Rg=4ohm (external)
23.2	11.8	92.5	3.9	VDS=380V VGS=10V ID=10A Rg=4ohm (external)

There is no significant difference in the measured Id current at max 20A or 10A For switching.

Maximum frequency is 380kHz at 50% duty cycle. (Safety Ratio is not applied in this case)



2.5 Gate Charge Characteristics and Body Diode Characteristics

($T_J=25^{\circ}\text{C}$) ⚡ :temperature dependent

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	

Gate charge characteristics

Gate to source charge	Q_{gs}	$V_{DS}=480\text{V}, I_D=20\text{A}, V_{GS}=10\text{V}$	-	8	-	nC
Gate to drain charge Affect to switching characteristic	Q_{gd}		-	19	-	
Gate charge total Affect to drive loss by Gate voltage	Q_g		-	59	-	
Gate plateau voltage	$V_{plateau}$		-	4.2	-	V

Reverse Diode (Body diode between source and Drain)

Continuous forward current as source current This is Body diode Forward current as Max.	I_S	$V_{GS}=0\text{V}$	-	-	20	A
Diode forward voltage ⚡ Voltage when forward current flow in body diode.	V_{SD}	$V_{GS}=0\text{V}, I_S=I_F$	-	0.9	1.2	V
Reverse recovery time ⚡ Time to disappear reverse recovery current.	t_{rr}	$V_{RR}=480\text{V}, I_S=I_F, d_{IF}/d_t=100\text{ A}/\mu\text{S}$	-	358	-	ns
Reverse recovery charge Charge to disappear reverse recovery current	Q_{rr}		-	6.8	-	μC
Peak reverse recovery current	I_{rm}		-	43.1	-	A

Source-Drain Diode Forward Voltage

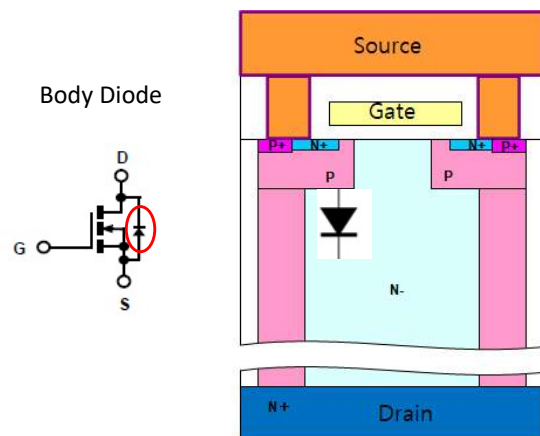
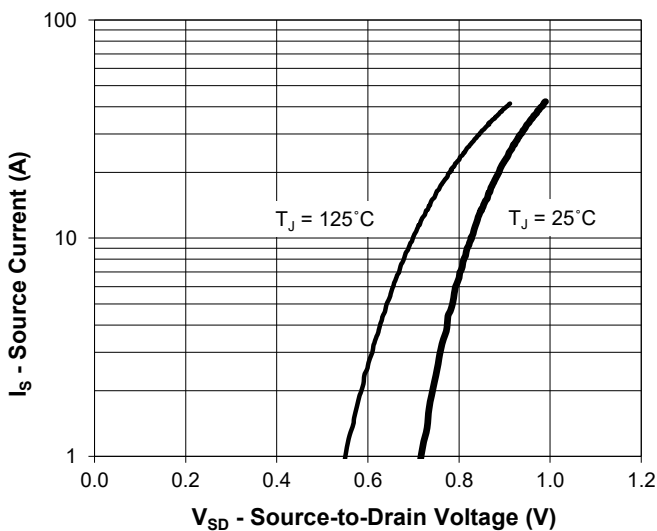


Fig.22 V_{SD} vs I_S as IF of Body Diode

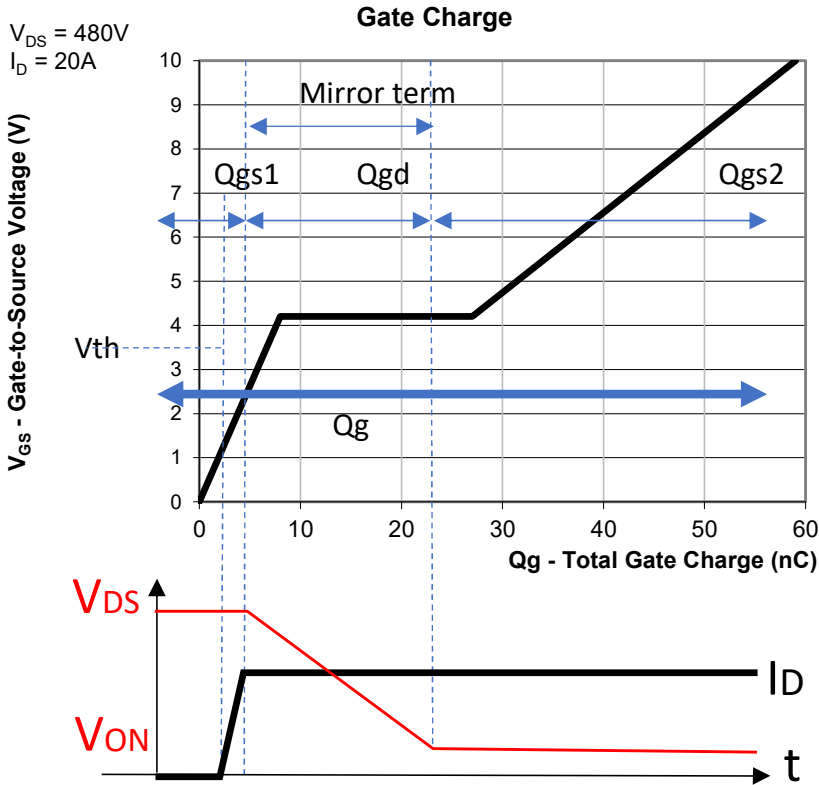


Fig.23 Gate Charge
 $Q_{gs} = Q_g - Q_{gd}$
 $Q_{gs} = Q_{gs1} + Q_{gs2}$

When a constant current is applied to the Gate, the Gate Voltage rises and the MOSFET turns ON. Charges are charged between Gate and source, and Gate and Drain during the mirror term. Total Gate Charge Q_g is give by Total Gate Current x Time.

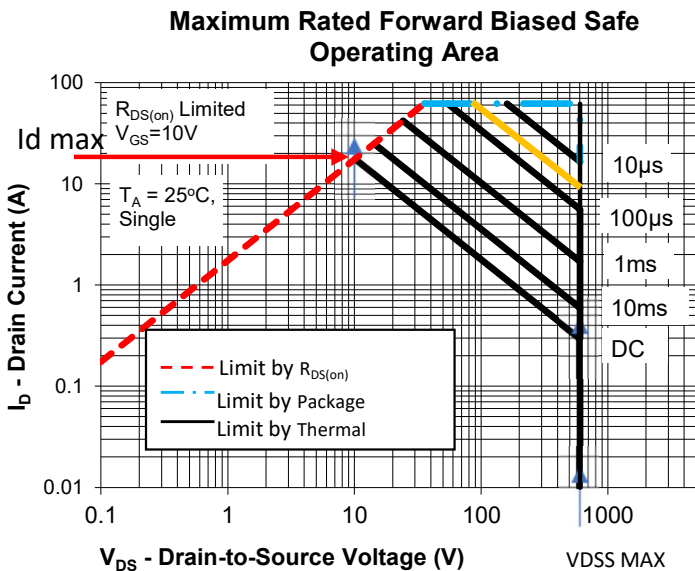
Lower Q_g correlates to less Gate drive losses.

FOM :Figure Of Merit is used as a performance index for Power MOSFETs.

$$FOM = R_{DS(on)} \times Q_g \quad (\Omega \cdot nC)$$

A Lower FOM is superior.

2.6 Safe Operating Area (SOA)



This figure is based on a temp=25°C
 Illustrating that the SOA range narrows as the case temperature T_c rises.

Example: Pulse=10µsec, $T_c=75\text{degC}$ to estimate SOA

$$\text{Derating Rate } D = (150 - T_c) / 125 \cdot 100$$

For the point, $16A \cdot 600V = 9600W$,

$$D = 0.6 \quad P_d(75) = P(25) \cdot D \\ = 9600 \times 0.6 \\ = 5580W$$

Therefore, the Yellow line could be SOA area for 10µsec, $T_c=75\text{degC}$

Fig.24 Safe Operating Area

Product shall be used within I_{dmax} , $R_{DS(ON)}$, Package and BVDSS

2.7 Transient Thermal Response

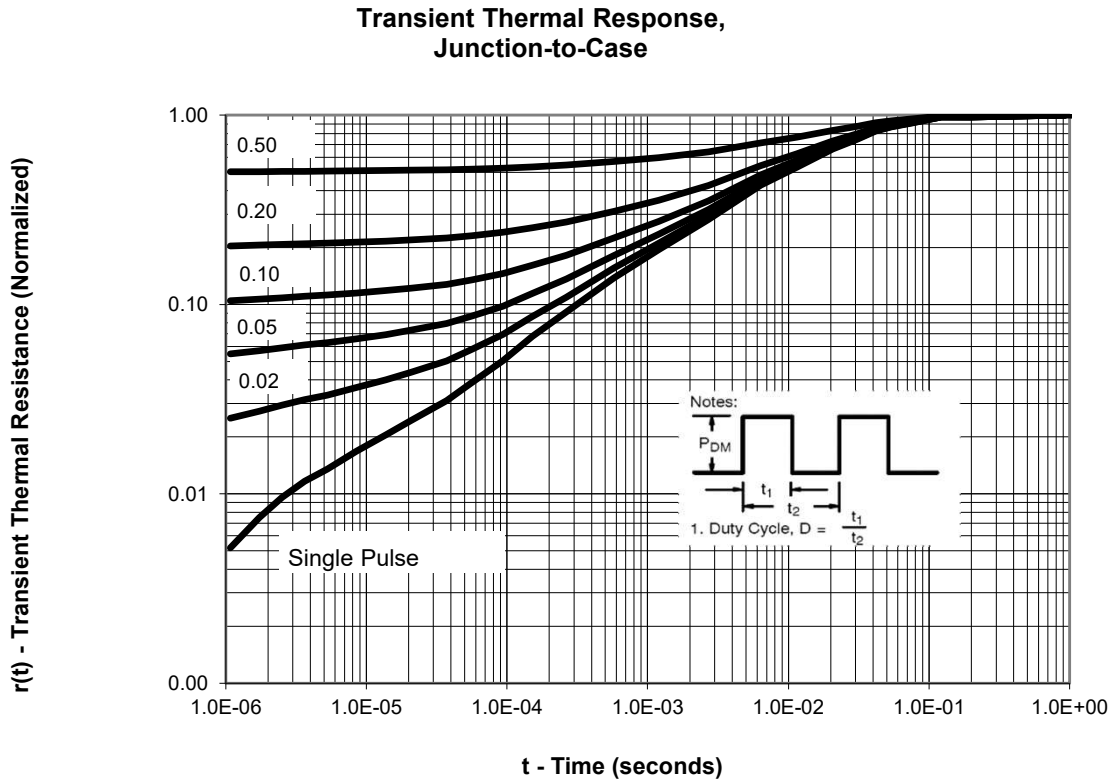


Fig.25 Transient Thermal Resistance $r(t)$ -pulse width time

t_1 =Pulse Width= PW

t_2 =Total Time

Duty= t_1/t_2

To calculate Channel temperature increasing ΔT_{ch} , refer to Fig24 for value of $r(t)$. $\Delta T_{ch}=P*r(t)$

Example 1 Pulse width t_1 $PW=10ms$, $D=0.2$ (Duty Cycle=20%)

How much temperature is increased when Power consumption= $60W$?

From the graph, $10ms$ with $D=0.2$ is for $r(t)=0.6$ 、 $R_{thjc}=0.69degC/W$

$$\Delta T_{ch}=P*r(t)=60*0.6*0.69=24.84^{\circ}C$$

Example 2 Condition: $T_c=85^{\circ}C$, Power= $40W$, Pulse Time= $10ms$, Single Pulse

How much temperature of T_j ?

$T_c=85degC$, $R_{thjc}=0.69degC/W$, $P=40W$,Duty=0, $r(t)=0.5$

$$\Delta T_{ch}=P*r(t)=40*0.5*0.69=13.8^{\circ}C$$

$$T_j=T_c+P*r(t)=85+(40*0.5*0.69) =98.8^{\circ}C$$

Example 3 Condition: $T_c=85^{\circ}C$,Frequency= $2kHz$,Duty Cycle=20%,

Peak Power= $50W$, How much temperature of T_j ?

$T_c=85degC$, $R_{thjc}=0.69degC/W$, $P=50W$,Duty=0.2, $f=2kHz$

$r(t)=0.24$ Pulse width=Duty* $1/f=0.2/2000=1E-4sec$

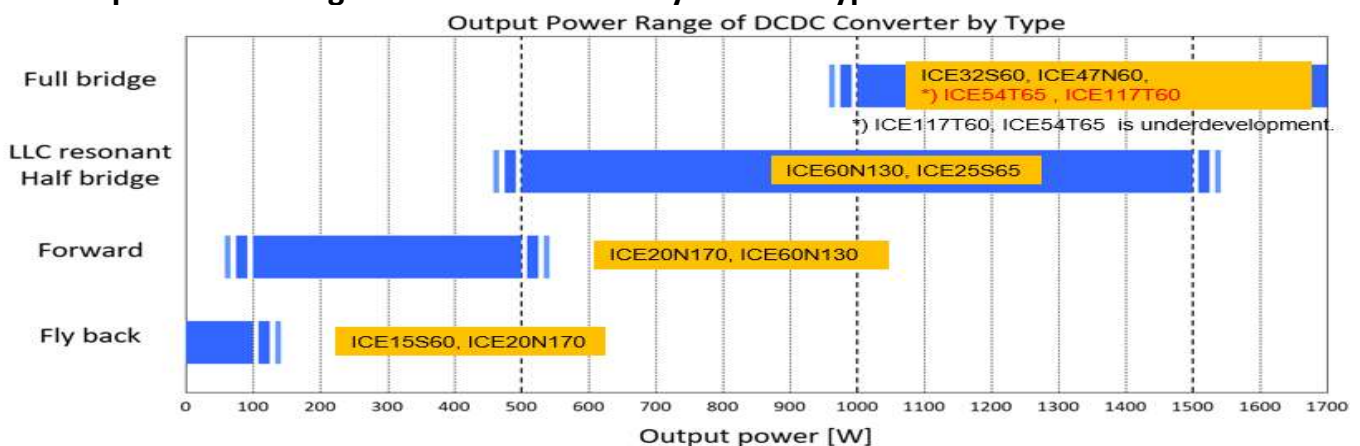
$$T_j=T_c+P*r(t)=85+(50*0.24*0.69) =93.28^{\circ}C$$

3. Product Family

3.1 Product List

GEN	Product	BVDSS Min. (V)	ID Max. (A)	RDSON Max. (Ω)	Qg Typ. (nC)	FOM ($\Omega \cdot$ nC)	IAR (A) Avalanche Current	Package *Pbfree TO=TO220* FP=Full Pak* W=TO247* D=TO252 L=DFN88 ,LK=DFN56 B=TO263 T=TOLL C=Wafer*
1	ICE47N60	600	47	0.068	189	12.85	20	W,C
	ICE60N130	600	25	0.15	84	12.60	11.5	TO,FP,W,C,B
	ICE22N60	600	22	0.16	84	13.44	11	TO, B ,W, T
	ICE20N170	600	20	0.199	59	11.74	10	TO,FP,W,C,B,T
	ICE20N60	600	20	0.19	59	11.21	10	TO,FP,W,B,C,T
	ICE19N60	600	19	0.22	59	12.98	9.5	L8x8
	ICE15N73	730	15	0.35	75	26.25	7.5	TO,FP,W , T
	ICES15N60	600	15	0.24	52	12.48	9.5	TO,FP,L8x8,B,T
	ICE13N60	600	13	0.27	48	12.96	9	TO,FP,L8x8,B,T
	ICE11N70	700	11	0.25	84	21.00	5	TO,FP,W,B,C ,T
	ICE10N60	600	10	0.33	43	14.19	5	TO,FP,W,B,L8x8,T
	ICES10N60	600	10	0.36	40	14.40	7	D
2	ICE32S60	600	32	0.078	47	3.67	10	TO,FP,W,C,T
	ICE25S65	650	25	0.133	34	4.52	8	TO,FP,W,C,B, T
	ICE24S65	650	24	0.141	34	4.79	8	L8x8
	ICE15S60	600	15	0.175	30	5.25	5	TO,FP,W,C,B ,T
	ICE14S65	650	14	0.195	24	4.68	5	TO,FP,W,C,B ,T
	ICE8S65	650	7.8	0.4	11.5	4.60	2.7	TO,FP,W,B,C,D,LK56,T

3.2 Output Power Range of DCDC Converter by Product Type



Circuit choice may be different depending on the output power. Full bridge may have over 1700W Power therefore please select the appropriate product depend on the power range. For example, the case of 100W Fly back , we offer ICE20N170 for Max Id=20A or ICE15S60 for Max Id=15A.

4. Applications

4.1 “Where used” Application Matrix

★: Displays the circuit used for each application

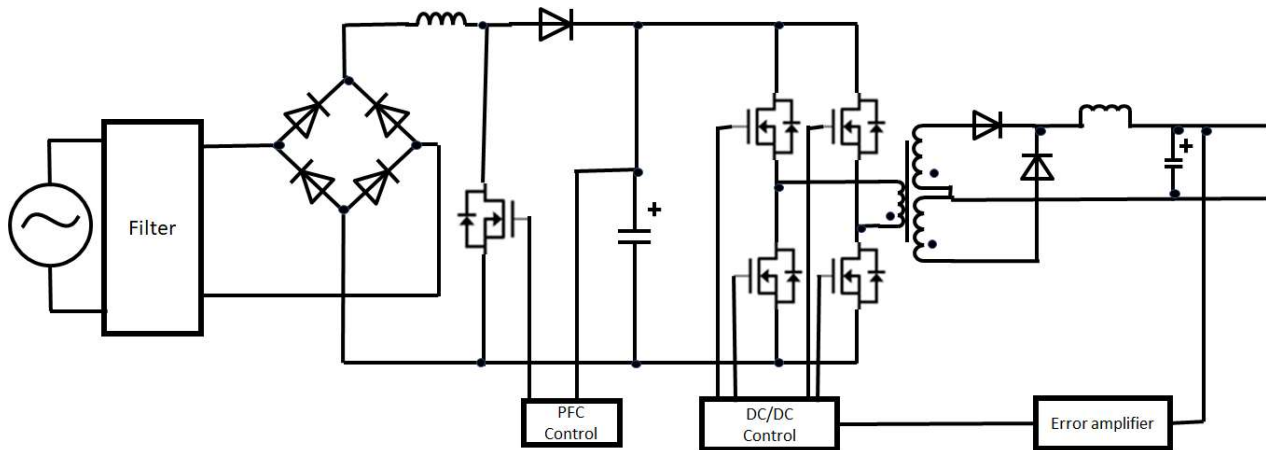
#	Application	Output Power (W)		Circuit								ICEMOS PART #
				AC-DC			DC-DC				DC-AC	
		Min	Max	Half Wave	Full Wave1	Full Wave2	Flyback	Forward	LLC Half Bridge	Full Bridge	Inverter	
a1	SMPS Power Factor Correction	500							★	★		ICE25S65 ICE60N130
a2	LLC Half Bridge	1000								★		ICE47N60 ICE32S60
b	Low Power SMPS Quasi- Resonant Flyback		100				★					ICE15S60 ICE20N60 ICE22N60W
c	High Power SMPS LLC Half- Bridge	500	1500						★			ICE47N60 ICE32S60
d	ATX Power Supplies	200	1600	★	★	★	★	★	★			ICE47N60 ICE32S60
e1	LED TV (140 Inch)	5k				★				★		ICE117T60 ICE47N60
e2	LED Lighting	20	500	★	★	★	★	★				ICE25S65 ICE60N130
f	Data Center AC/DC (Severs & Telecom)	500k-1k node				★				★		ICE117T60 ICE47N60
g	Fast Chargers	3k	400k			★				★		ICE117T60 ICE47N60
h	Chargers PC Adapters	36	90	★	★		★					ICE15S60 ICE10N60 ICE19N60L
i	TV Power Application	24	410		★	★	★	★				ICE25S65 ICE60N130
j	UPS	500	10k			★			★	★	★	ICE117T60 ICE47N60
k	Solar Inverters	300	6k					★	★	★	★	ICE117T60 ICE47N60
l	HID Street Lights	22	500			★		★	★			ICE25S65 ICE60N130
m	Gaming Consoles	100	200		★	★		★				ICE60N130 ICE19N60L
n	LED Signage	10	250	★	★			★				ICE60N130 ICE20N170
o	E-Bikes/E-Mobility	600	40k			★			★	★		ICE117T60 ICE47N60
p	Printers	10	1500	★	★	★	★	★	★	★		ICE10N60FP ICE20N60FP ICE47N60
q1	White Goods Fridge	200	300			★			★	★	★	ICE60N130 ICE20N170
q2	Washing Machine	800	1500			★			★	★	★	ICE117T60 ICE47N60
r1	Audio Amp	200 x n	5k x n			★			★	★		ICE117T60 ICE47N60
r2	Projector	300	2k			★		★	★	★		ICE47N60 ICE8S65FP
s1	Car audio	10 x n	100xn				★	★				ICE47N60 ICE32S60
s2	Navigation	10	20				★					ICE15S60 ICE19N60L
u	3D printer	180	1500	★	★	★	★	★	★	★		ICE117T60 ICE47N60
v	Smart Phone Adaptors	20	90	★	★		★					ICE15S60 ICE20N170
w	Industrial Power Supply	320	1300			★			★	★		ICE117T60 ICE47N60
x	Tablet/Laptop	200	1500	★	★		★					ICE15S60 ICE20N170
y	Micro Inverters	200	1500						★	★	★	ICE117T60 ICE47N60

4.2 Circuits

4.2.1 Full Bridge Converter (Isolated)

Example of Server Management

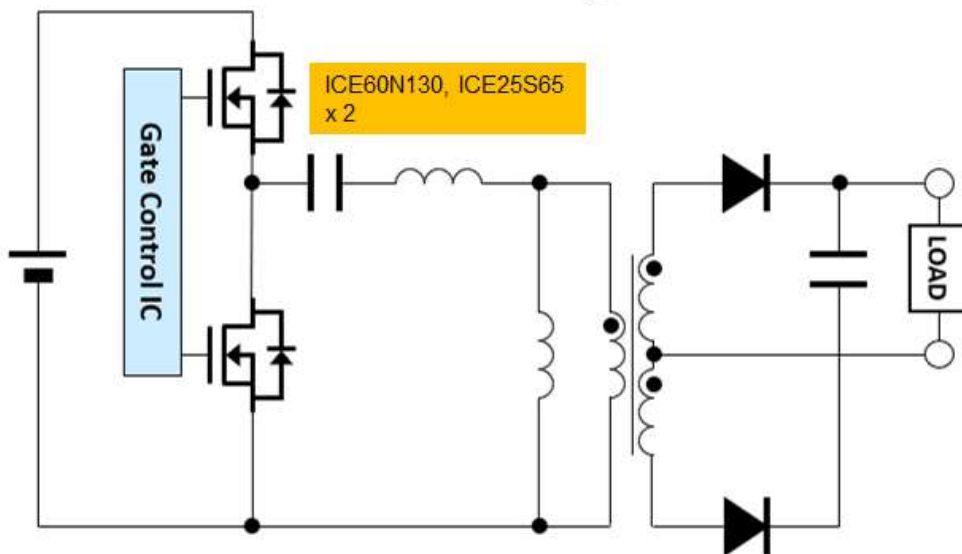
ICE32S60, ICE47N60, ICE117T60 x 4



4 pieces used of ICE47N60 or ICE32S60

4.2.2 LLC Resonant Half Bridge Converter (Isolated)

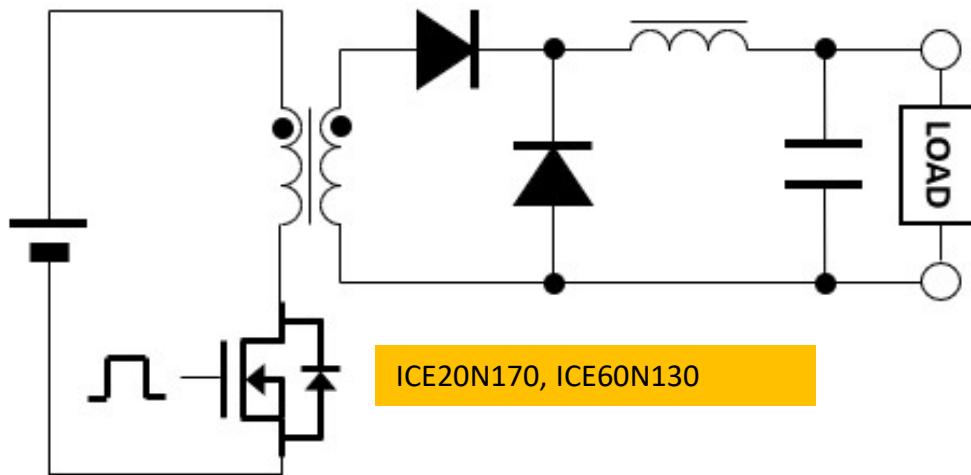
LLC Resonant Half Bridge Converter



2 pieces used of ICE60N130 or ICE25S65

4.2.3 Forward Converter (Isolated)

Forward converter

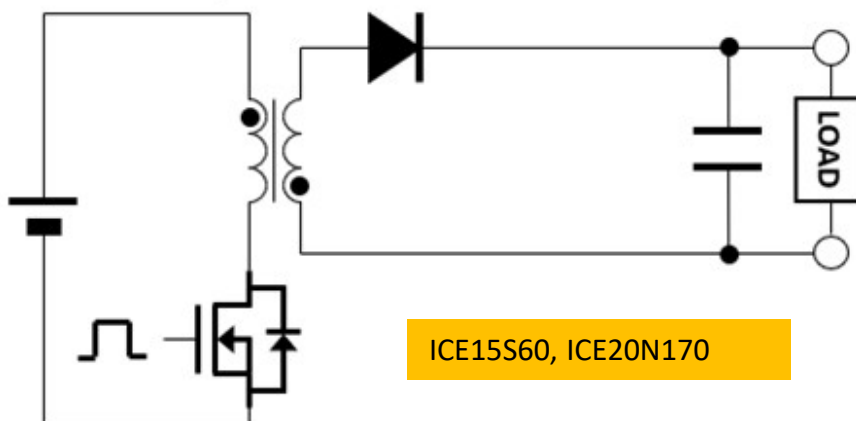


1 piece used of ICE20N170 or ICE60N130

This system can supply a wide range of power. Compared to the flyback converter an additional diode and choke coil are required but the ripple voltage is lower. The output voltage is determined by the ratio of the number of turns on the primary and secondary sides.

4.2.4 Flyback converter (isolated)

Flyback converter



2 pieces used ICE15S60 and ICE20N170

Since the ripple voltage is larger compared to the other converters, a larger capacitor is required. The output voltage is determined by the ratio of the number of turns on the primary and secondary sides.

5. Failure Modes of Power MOSFETs.

There are 3 main failure modes as below:

5.1 Avalanche Failure (UIS failure)

The device will be destroyed by a voltage / current load that exceeds the E_{AS} capacity to withstand when switching off, such as in an L load circuit. Phenomenon such as $V_G(th)$ deterioration and short circuit between drain and source are confirmed. It is also necessary that the channel temperature T_j in the avalanche state is 150°C or less.

5.2 EOS Failure (Electrical Over Stress outside SOA or beyond Voltage or Current)

When devices experience stresses beyond their safe operating range such as voltage surge, excess current or thermal stress resulting in a damaged device. In this mode metal burn marks can be visible over die surface and the silicon might be melted. The three 3 pin terminals(Gate-Drain-Source) could short circuit. Our product has been tested to failure by a Class 2 1000V Voltage Surge from a IEC61000-4-5 Surge Generator resulting in burn marks around the Gate and Source pads.

5.3 ESD Failure(Electro-static Discharge)

Our SJMOSFET ESD capacity is classified by MIL-STD-1686 as below:

Human Body Model Class 3 (4000-15999V)

Machine Model Class M5 > +-800V

ESD can cause problems such as gate leaks due to polysilicon or gate oxide film destruction, and resistance shorts between drain and source. When handling, ESD such as 1MΩ grounding and applying Anti static Discharge action to the Equipment.

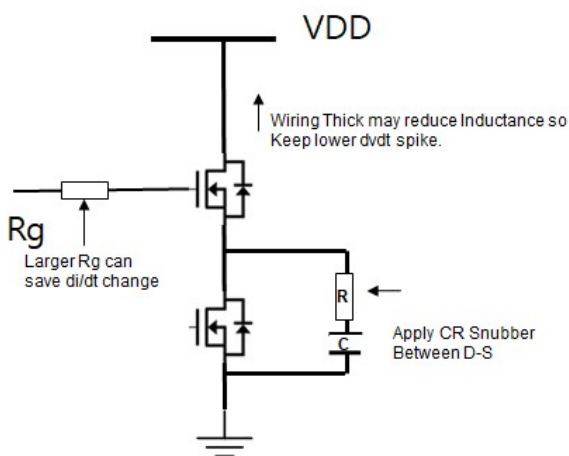


Fig.26 Measure to prevent Body Diode breakage

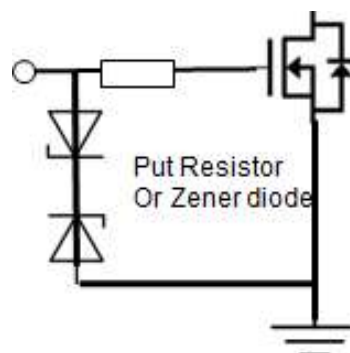


Fig.27 Measure to prevent ESD failure

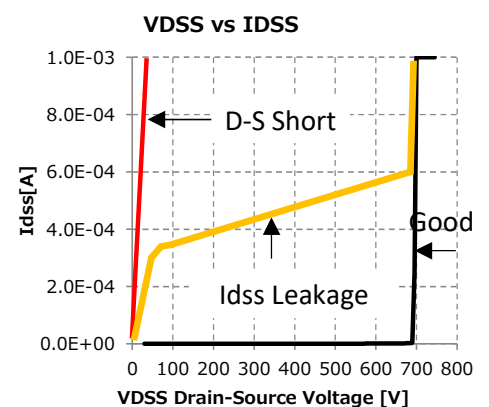
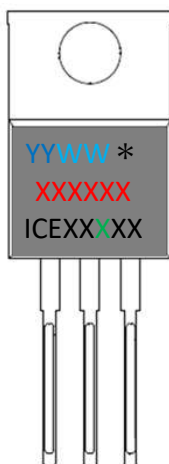


Fig.28 Example of characteristic DC failure

6. Reliability Test Results

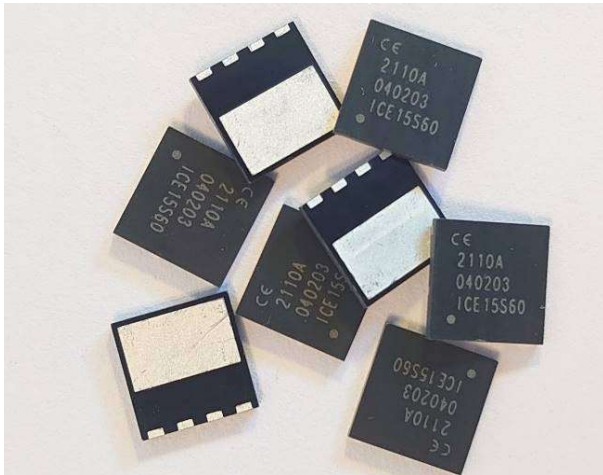
Items	Test Description(Abbr.)	Test method.	Stress Condition	Result
1	Temperature Cycle(TCT)	JESD22-A104	1000 cycles, ΔT_j -55 to 150°C	PASS
2	High Temp storage(HTS)	Mil-Std. 750 Method 1032	500 hrs, $T_j = 150^\circ\text{C}$	PASS
3	Steady State Gate Bias positive (HTGB)	Mil-Std. 750 Method 1042-B	1000 hrs, $V_{GS} = +24\text{V}$ $T_j = 150^\circ\text{C}$	PASS
4	Steady State Gate Bias negative (HTGB)	Mil-Std. 750 Method 1042-B	1000 hrs, $V_{GS} = -24\text{V}$ $T_j = 150^\circ\text{C}$	PASS
5	Steady State Reverse bias (HTRB)	Mil-Std. 750 Method 1042-A	1000 hrs, $V_{DS} = 80\% \text{ BVDSS}$ $T_j = 150^\circ\text{C}$	PASS
6	High Temp High Humidity Reverse Bias (H3TRB)	Mil-Std. 750 Method 1042-A	1000 hrs, $V_{DS} = 480\text{V}$ $T_j = 85^\circ\text{C}$, $\text{RH} = 85\%$	PASS
7	Pressure Cooker Test (PCT)	Method JESD22-A102	121C 100% RH, 205Kpa,96 hours	PASS
8	Highly Accelerated stress test (HAST)	JESD22-A110D	130°C 85% RH, 230Kpa, 96 hours	PASS
9	Resistance to Solder Heat Test (RSH)	JESD22- B106(PTH)	265°C 10-12secs 3 cycles	PASS
10	Solderability	JESD22-B102E	260°C 10 secs	PASS

7. Device Marking Format

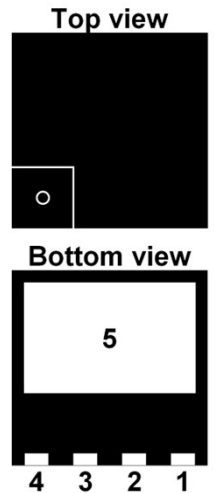
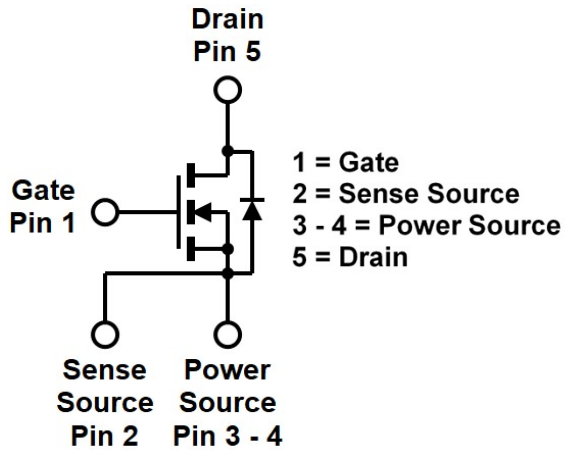


YY=Last two digit in Year
 WW=Work Week
 * Manufacturing site ID
 XXXXXX =Production lot ID
 ICEXX XX =ICEMOS Product name
 X=N : GEN1 , S : GEN2, T :GEN3

8. DFN 8X8 information



DFN 8x8 Leadless Package



DFN8x8

Features:

- Low On-resistance
- Ultra Low Gate Charge
- High peak current capability
- High dv/dt capability
- Tape & Reel packaging (13-inch reel)
- 3,000 units per reel size
- Eco-Friendly, MSL-1

Applications:

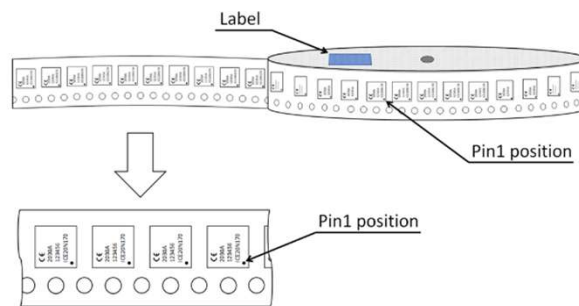
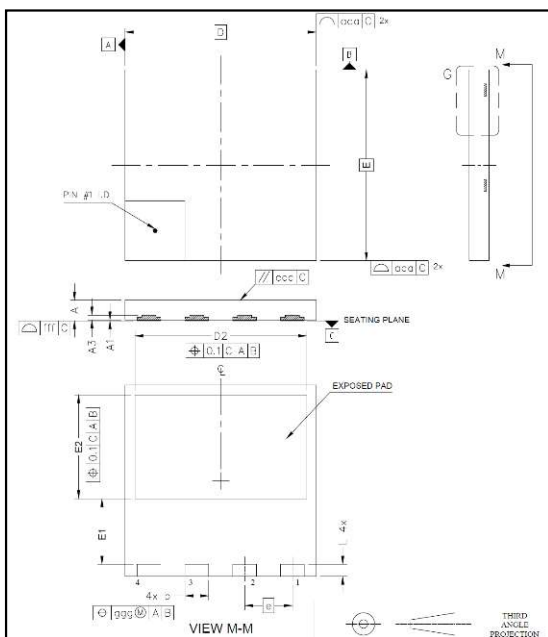
- ◆ Servers
- ◆ Adapters
- ◆ HID Lighting
- ◆ UPS
- ◆ Renewable Energy

Benefits:

- ✓ Ideal For High Density Applications
- ✓ Ideal For High-Speed Automated Production
- ✓ Low Profile Leadless Package

Part Number	GEN1	GEN2	GEN2
	ICE19N60L	ICE15S60L	ICE25S65L
Polarity	N	N	N
Id(Max)	19A	15A	25A
V(BR)DSS (Min)	600V	600V	650V
Rds(on) (Typical)	0.20 Ω	0.155 Ω	0.120 Ω
Qg (Typical)	59nC	30nC	34nC
FOM(ΩxnC)	11.8	4.65	4.08

Release plan is early Q3 on GEN1, Q4 on GEN2



SYMBOL	MIN	MAX	NOTES
A	0.75	0.95	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
A1	0.00	0.05	
A3	0.10	0.30	2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
b	0.90	1.10	
D	7.90	8.10	3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.90mm AND 1.10mm FROM TERMINAL TIP.
E	7.90	8.10	
D2	7.10	7.30	4.0 DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
E1	2.65	2.85	
E2	4.25	4.45	5.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
e		2.00 DSC	
L	0.40	0.60	6.0 RADIUS ON TERMINAL IS OPTIONAL.
aaa		0.10	
bbb		0.05	
ccc		0.05	
fff		0.05	




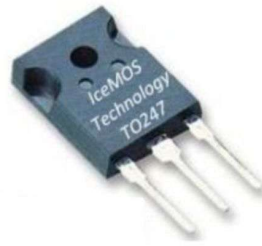
9. PACKAGE information



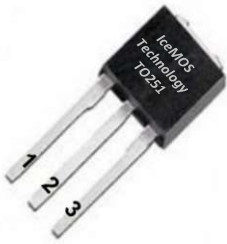
TO220  Lead Free



TO220FP  Lead Free
Full Pak



TO247  Lead Free



IPAK  Lead Free
TO251



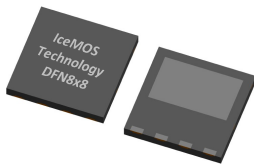
I2PAK  Lead Free
TO262



D2PAK
TO263-2L
(MSL3)



DPAK
TO252
(MSL3)



DFN8x8
(MSL3)



DFN5x6
(MSL3)



TOLL
(MSL3)

Leadless Package Shipping Information

Package Type	Packing	MOQ
DFN 5x6	Tape & Reel	3,000 pcs
DFN 8x8	Tape & Reel	3,000 pcs
TOLL 8	Tape & Reel	2,000 cps

Leaded Package Shipping Information

Package Type	Packing	MOQ
TO-220	Tubes	50pcs
TO-220 Fullpak	Tubes	50pcs
TO-247	Tubes	30pcs
TO-263 (D2pak)	Tape & Reel	800pcs

Package:

- RoHS Directive (EU)2015/863
- Lead Free(Pb free) product.(except some of surface mount)
- Halogen Free
- Eco-Friendly Mold Compound



Our Pb free definition is no use of Pb for any device inside and outside.

~Guidelines for Handling our SJ MOSFET~

1. Soldering Temperature
Flow /Reflow : 260°CMax 10 sec 2 times
iron soldering : 380°CMax 3 sec 1 time
2. Shelf Life Guideline:
Packaged product 5 years Wafer form 3 years
3. Avoid sudden temperature changes and store at a Temp 5~35°C and a humidity of 20~75%RH The moisture Sensitive Level of TO220,TO220FP and TO247 is MSL1. DPAK,D2PAK,DFN8x8 and DFN5x6 is MSL3.
4. Please keep away from corrosive, chloride, excessive weight and direct sunlight as the product quality may degrade so please avoid these conditions for your storage.
5. To prevent damage from static electricity (ESD) store the product in an ESD-resistant package. When handling the device ground the jig, device, bench etc.
6. Our products comply with RoHS and REACH. We do not use any minerals from conflict zones

Contact:

IceMOS Sales: sales@icemostech.com

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