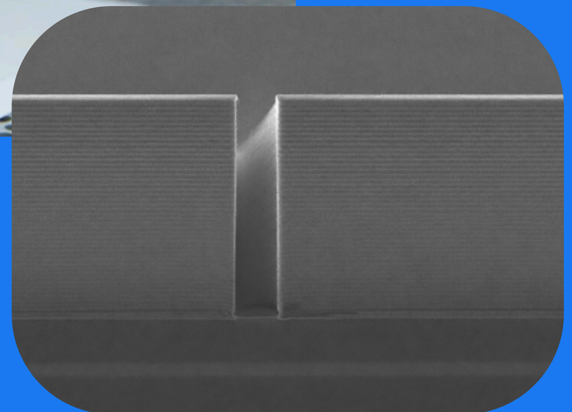
IceMOS Technology

SOI WAFERS

ADVANCED ENGINEERED SUBSTRATES

MEMS SENSING ELEMENTS



www.icemostech.com

About IceMOS

IceMOS Technology is a global semiconductor leader operating a proprietary fabrication facility in Western Europe. We deliver advanced Engineering Substrates that drive millions of smart, connected applications, transforming the way people work and live. Our substrates enhance speed, efficiency, and reliability across microelectronics, power devices, MEMS sensors, and photonics.

About IceMOS

- **MEMS** sensing element and Advanced Substrates fabrication and R&D
- **Location**: Belfast, Northern Ireland, UK.
- **Size**: 25,000 sq ft facility
- **Capacity**: 15,000 wafer starts/month in a mix of 100, 125, 150, and 200mm diameter wafer sizes.
- **Production**: 4 cleanrooms range from Class-10 to Class 10,000.
- **Automotive** dies shipped: >200M, with ZERO field failures.

IceMOS Technology

SOI Wafers

Bonded Silicon-on-Insulator Wafers

Example Applications:

- Advanced pressure sensors
- Accelerometers
- Gyroscopes
- Microfluidics/flow sensors
- RF MEMS
- MOEMs/Optical MEMs
- Optoelectronics
- Smart Power
- Advanced Analog ICs
- Microphones
- Luxury watches

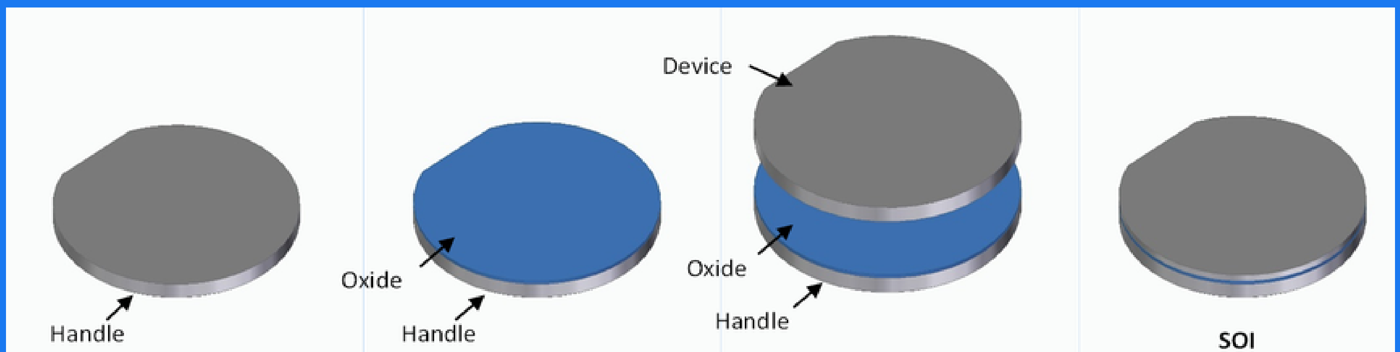
End Markets:

- Telecommunications
- Medical
- Automotive
- Consumer
- Instrumentation

IceMOS is a leading supplier of 100–200 mm thick-film SOI wafers for a wide range of IC and MEMS applications. With more than 22 years of experience in SOI manufacturing, we offer a specification range that is among the broadest available on the market.

Our extensive expertise across a variety of SOI substrates, combined with our highly skilled applications engineering team, enables us to help customers select the optimum combination of parameters for their specific requirements. This ensures the delivery of a fully customised SOI solution tailored to each application.

Through continuous process improvements within a Lean Six Sigma environment, IceMOS Technology delivers world-class product quality, a competitive cost structure, and rapid turnaround times — making us the ideal SOI partner.



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SOI Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150 mm	200 mm
Handle Layer Specifications		
Handle Thickness	200–1100 µm	450-1100 µm
Handle Thickness Tolerance	±5 µm	
Stack Thickness	≥280 – ≤1150 µm	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Backside Finish	Lapped/Etched or Polished	
Buried Oxide Specifications		
Thermally Oxidised Buried Oxide Thickness	0.2 – 4.0 µm grown on Handle, Device or both wafers	
Device Layer Specifications		
Device Layer Thickness	≥1.5 µm	5-300 µm
Tolerance	± 0.5 µm	±0.8 µm
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Buried Layer Implant	N type or P type	

The specifications shown above represent standard IceMOS Technology offerings; however, we are always pleased to work closely with customers to develop tailored solutions for specific application requirements. To discuss an alternative specification, please contact our sales team at **sales@icemostech.com**

IceMOS Technology

SiSi Wafers

Bonded Silicon-Silicon Wafers

Example Applications:

- Advanced pressure sensors
- AHigh Voltage PIN Diodes
- RF Attenuators
- Photo Detectors
- X-Ray Detectors
- IR Sensors
- HV Power Devices
- Replacement for Epitaxial layers

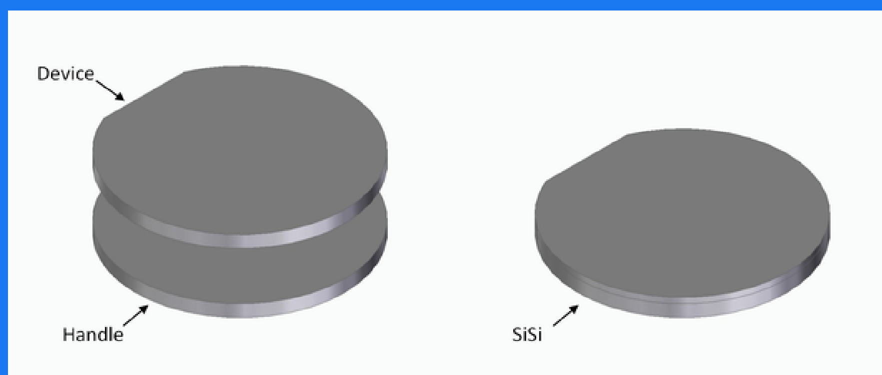
Key Features:

- High Quality
- Low cost
- Low defect density
- Excellent Layer uniformity
- Multiple layers
- Sharp transitions
- Layer resistivity up to 10 kW-cm
- Excellent interface quality – verified by high resolution SAM Inspection

For semiconductor device manufacturers, the IceMOS Silicon–Silicon direct bonded wafer provides a cost-effective alternative to the thick epitaxial layers and inverse epitaxy traditionally used in applications such as power devices and PiN diodes.

By using direct wafer bonding technology, silicon substrates can be produced with multiple layers of single-crystal silicon. These layers can offer resistivity values ranging from 1 mΩ-cm to 10 kΩ-cm, in both N-type and P-type configurations, and can include combinations of crystal orientations — a capability not achievable with conventional epitaxial wafers.

The IceMOS SiSi bonding process delivers high-quality wafers with low leakage current, minimal warp, and low defect density. In addition, layer thickness variation can be controlled to as little as ±0.5 µm. The transition between high and low dopant concentrations can be engineered to be either sharp or gradual, depending on the application and customer requirements.



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SiSi Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150 mm	200 mm
Handle Layer Specifications		
Handle Thickness	200–1100 µm	450-1100 µm
Handle Thickness Tolerance	±5 µm	
Stack Thickness	280–1150 µm	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Backside Finish	Lapped/Etched or Polished	
Device Layer Specifications		
Device Layer Thickness	≥1.5 µm	≥5 µm
Tolerance	± 0.5 µm	±0.8 µm
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Buried Layer Implant	N type or P type	

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IceMOS Technology

DSOI Wafers

Bonded Double/ Multi-Layer SOI Wafers

Example Applications:

- SOI solutions for MEMS/MST
- Microfluidics/flow sensors
- RF MEMS
- MOEMs
- Optoelectronics
- Optical MEMS

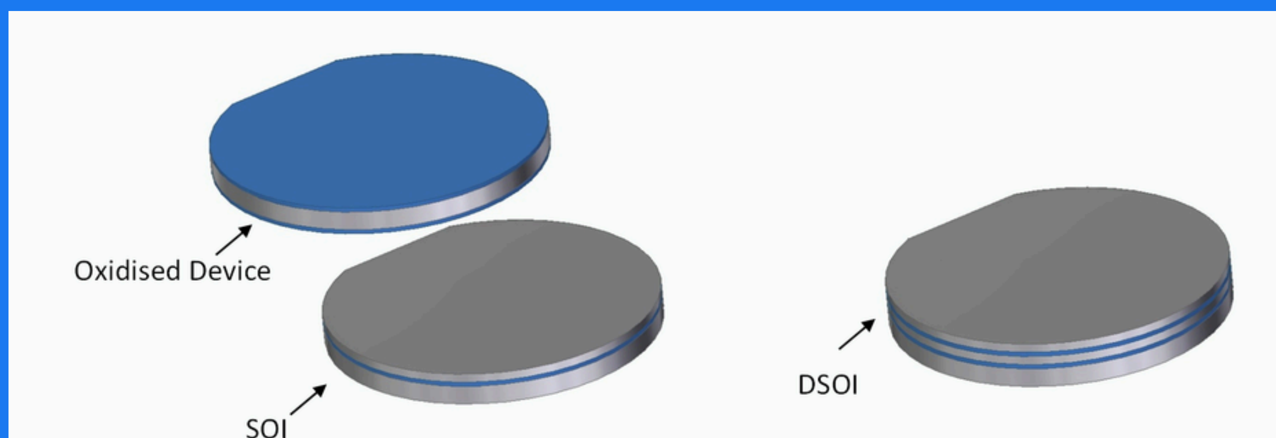
End Markets:

- Telecommunications
- Medical
- Automotive
- Consumer
- Security

IceMOS is a leading supplier of Double and Multi-Layer SOI wafers for a wide range of IC and MEMS applications. With extensive experience, we offer one of the broadest specification ranges on the market, delivering optimised DSOI solutions tailored to your application requirements.
Our expertise in SOI substrates and applications engineering helps customers select the ideal parameter combination to support downstream processing .

From small-volume R&D production to high-volume manufacturing, IceMOS provides a flexible and scalable approach.

Operating within a Lean Six Sigma environment, IceMOS Technology continuously enhances its processes to deliver world-class quality, cost-effective solutions, and fast turnaround times — making us a trusted multi-layer SOI partner.



DSOI Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150 mm	200 mm
Handle Layer Specifications		
Handle Thickness	200–1100 µm	450-1100 µm
Handle Thickness Tolerance	±5 µm	
Stack Thickness	280–1150 µm	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Backside Finish	Lapped/Etched or Polished	
Buried Oxide Specifications		
Thermally Oxidised Buried Oxide Thickness	0.2 – 4.0 µm grown on Handle, Device or both wafers	
Device Layer Specifications (1st and 2nd Layer)		
Device Layer Thickness	≥1.5 µm	≥5 µm
Tolerance	± 0.5 µm and ± 1 µm	±0.8 µm and ± 1.6 µm
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Buried Layer Implant	N type or P type	

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IceMOS Technology

DSP Wafers

Double-Side Polished Silicon Wafers

Example Applications:

- DSP solutions for MEMS/MST
- Microfluidics/flow sensors
- RF MEMS
- Optoelectronics

End Markets:

- Telecommunications
- Medical
- Automotive
- Consumer
- Security

IceMOS uses over 22 years of experience to offer the marketplace world class custom DSP solutions (Double Sided Polished).

Our highly skilled team has many years of design and manufacturing experience to help develop a DSP solution to your requirement.

IceMOS DSP wafers are an excellent substrate for double sided lithography processing; the IceMOS expertise and knowledge of the product and the processes allow for exceptional thickness control and surface roughness – ideal for a downstream wafer bonding process. Additionally, non-standard specifications for demanding applications will always be considered.

Our world class product quality, competitive cost structure plus rapid turnaround makes IceMOS Technology your ideal DSP partner.

IceMOS Technology

DSP Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150mm	200mm
Wafer Thickness	300–1150 µm	450-1150 µm
Wafer Thickness Tolerance	±2 µm	±5 µm
Total Thickness Variation (TTV)	≤1 µm	≤2 µm
Bow	≤40 µm	
Warp	≤40 µm	
Roughness	≤2Å	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Thermally Oxidised Field Oxide Thickness	0.2-4.0 µm	

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IceMOS Technology

mCSOI™ Wafers

MEMS Cavity Bonded SOI Wafers

Example Applications:

- Advanced pressure sensors
- Inertial MEMS
- Microfluidics
- Resonators
- Microphones

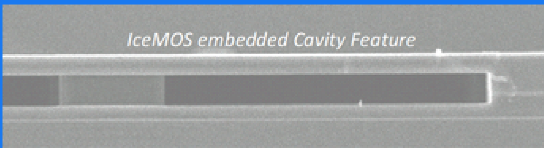
End Markets:

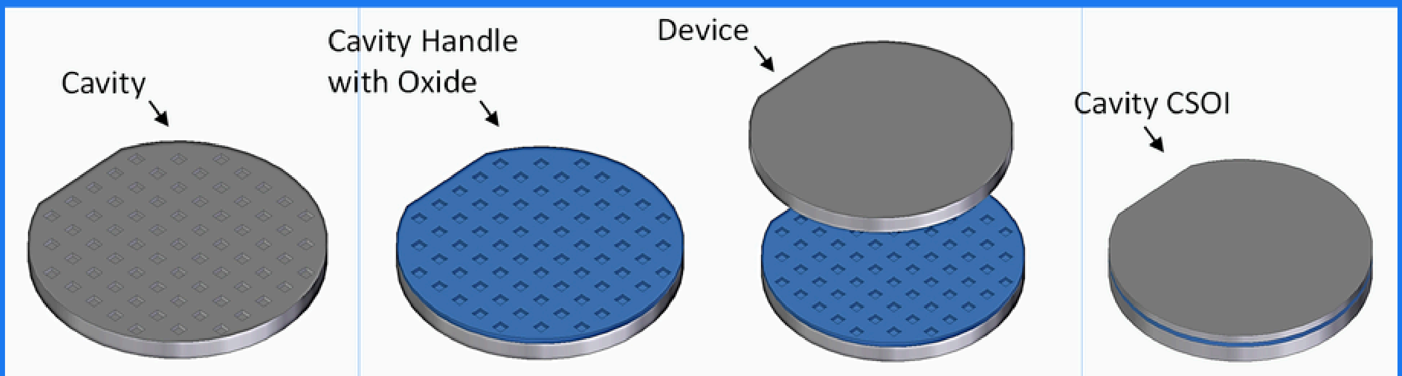
- Telecommunications
- Medical
- Automotive
- Consumer
- Instrumentation

IceMOS Technology is a leading supplier of Cavity Bonded SOI wafers for a wide range of MEMS applications. Combining advanced wafer bonding technology with extensive deep silicon trench etch expertise, IceMOS enables complex cavity structures to be integrated beneath silicon membranes, supporting the development of innovative, high-performance MEMS devices.

IceMOS Cavity Bonded SOI solutions provide several key advantages, including reduced stiction during release, low-cost SOI/Si-Si cavity solutions, simplified manufacturing flows, and flexible designs tailored to customer applications.

Multiple construction methods are available to optimise cavity performance, with optional SAM and AVI inspection services. Advanced integrated features can also be incorporated, enabling new design possibilities for next-generation MEMS applications.





IceMOS Technology

mCSOI Specification

Parameter	Specification Range
Wafer Diameter	100, 125, 150 mm
Handle Layer Specifications	
Handle Thickness	200–1100 µm
Handle Thickness Tolerance	±5 µm
Stack Thickness	280–1150 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Backside Finish	Lapped/Etched or Polished
Buried Oxide Specifications	
Thermally Oxidised Buried Oxide Thickness	0.2 – 4.0 µm grown on Handle, Device or both wafers
Device Layer Specifications	
Device Layer Thickness	≥1.5 µm
Tolerance	± 0.5 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Buried Layer Implant	N type or P type
Membrane Thickness/SOI Thickness	>2 µm
Membrane Tolerance	+/-0.5 µm
Cavity Span: Membrane Thickness	<50:1 µm (dependent on design)
Minimum Bonding Size Features	20 µm
Alignment Accuracy of Cavity to Alignment Marks	+/-3 µm
Cavity Depth	1-30 µm @ +/-10% 31-300 µm @ +/-20%
Cavity Location	Handle, Device or Buried Oxide

The specifications shown above represent standard IceMOS Technology offerings; however, we are always pleased to work closely with customers to develop tailored solutions for specific application requirements. To discuss an alternative specification, please contact our sales team at **sales@icemostech.com**

IceMOS Technology

mTSOI ™ Wafers

Deep Trench Isolation Bonded SOI Wafers

Example Applications:

- MEMS devices
- Solid State Relay photovoltaic generators
- Photovoltaic cells and Optoelectronic devices/ICs
- High Voltage Analog ICs
- High performance bipolar circuits
- Smart Power ICs
- Integrated Sensors

Key Features:

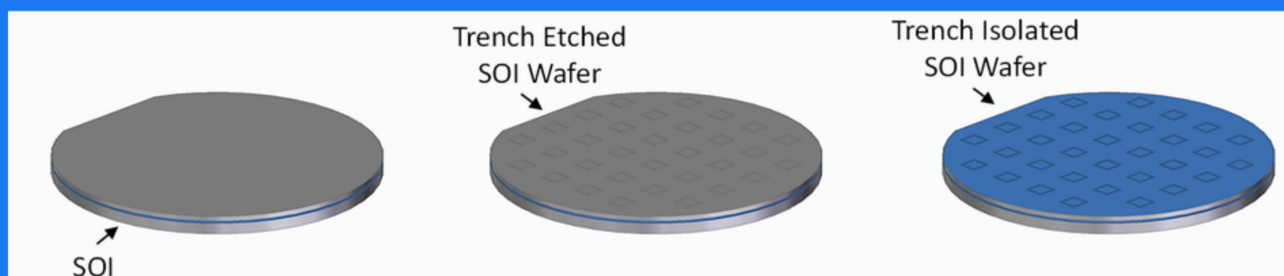
- Complete device isolation
- Allows significant die shrinkage compared with conventional Junction isolation
- Much lower defect density than conventional DI technologies
- Lower Substrate capacitance than bulk
- Lower cost than trench isolation on epi

IceMOS dielectric isolation technology delivers high voltage isolation between components on the same chip. Isolation is achieved using thick film SOI technology combined with state-of-the-art high aspect ratio deep trench etching and oxide/poly refill.

Supply Options Available:
· Provision of DI Substrate from isolation mask provided
· Provision of Fully processed DI IC using ICEMOS as foundry to complete post isolation processing
· Provision of Full IC design and fabrication on DI from customer schematic

The IceMOS trench-isolated silicon-on-insulator (SOI) substrate provides complete dielectric isolation of tubs.
Key benefits are:
· Elimination of buried layer
· Elimination of epi layer
· Elimination of P+ isolation diffusion
· Minimizing of parasitic capacitances
· High quality crystalline silicon layer
· Simultaneous increase of die per wafer
· High voltage breakdown capability
·Customised trench patterns

Our process engineers will work closely with your design group to realize the full potential for your processes.



IceMOS Technology

Trench SOI Specification

Parameter	Specification Range
Wafer Diameter	100, 125, 150 mm
Handle Layer Specifications	
Handle Thickness	350–800 µm
Handle Thickness Tolerance	±5 µm
Stack Thickness	350–1150 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Backside Finish	Lapped/Etched or Polished
Buried Oxide Specifications	
Thermally Oxidised Buried Oxide Thickness	0.2 – 4.0 µm grown on Handle, Device or both wafers
Device Layer Specifications	
Device Layer Thickness	1.5 - 100 µm
Tolerance	± 0.5 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Buried Layer Implant	N type or P type
Trench Mask Tone	Positive Resist
Trench Mask Type	E-beam master for projection aligner
Trench Line Width	> 2um
Trench Aspect Ratio	15:1
Trench Sidewall Doping Type	Phosphorus
Trench Refill – Oxide (each sidewall)	0.1 – 1.0 µm
Trench Refill – Polysilicon	To Fill (Doped or undoped Polysilicon)
Planarisation	CMP
Final Field Oxide	Thermal oxide + TEOS up to 1um

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TSV Wafers

Through Silicon Vias

Example Applications:

- SOI solutions for MEMS/MST
- Microfluidics/flow sensors
- RF MEMS
- Optoelectronics
- Smart Power
- Advanced Analog ICs

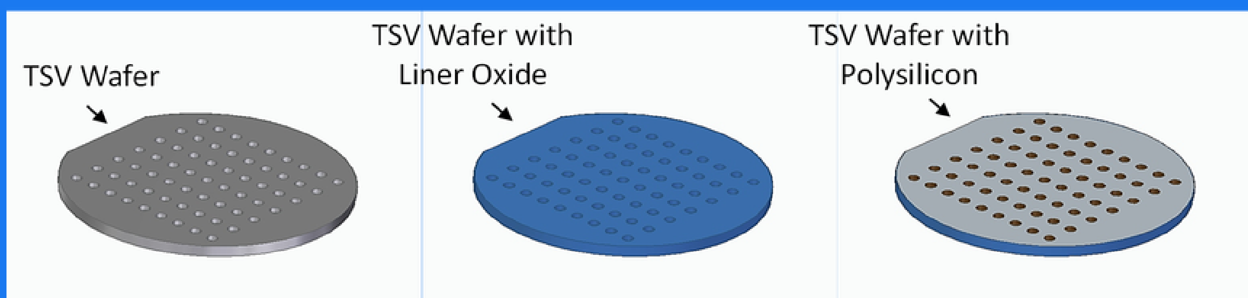
End Markets:

- Telecommunications
- Medical
- Automotive
- Consumer
- Instrumentation

IceMOS has developed an innovative through-wafer interconnect technology that helps designers in the standard IC and MEMS industries overcome packaging challenges. This solution enables customers to migrate designs easily to wafer-level packages with solder-bumped contacts.

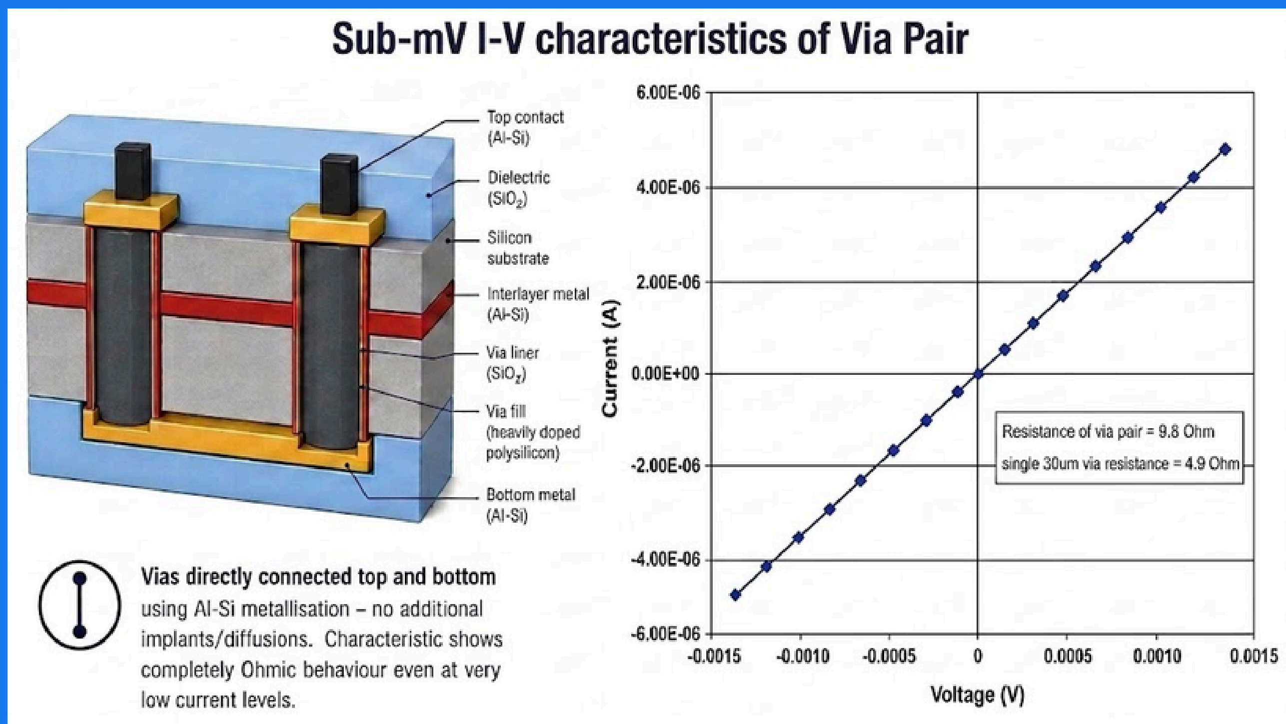
The IceMOS solution is a pre-processed substrate delivered with the interconnects already formed within the wafer. The substrate is fully CMOS-compatible.
All interconnects are created using through-wafer etching, refill processes, and heavily doped polysilicon. The wafers meet standard specifications for surface metallic contamination, planarity, and particle count. Stable substrate performance has been verified at diffusion temperatures up to 1200°C.

IceMOS develops customer-specific through-wafer interconnect solutions in partnership with customers, implementing preferred interconnect patterns directly on the wafer for easy connection to circuits or sensors. TSVs can be positioned beside or beneath existing bond pads. Each design is fully customised and optimised to meet customer requirements.



TSV Specification

Parameter	Specification Range
Aspect Ratio of Via	<15:1
Wafer Diameter	100mm & 150mm
Wafer Thickness	300-525μm
Max. Diameter	40μm on smallest side
Min. Pitch	90μm (3x via width)
Poly Resistivity	<5 mΩ-cm
Isolation Resistance	Determined by oxide liner (design dependent)
Oxide Liner Thickness	0.2-2μm



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IceMOS Technology

Foundry Services

Key Features:

- High Quality
- Low cost
- Low defect density
- Multiple layers
- Process sequences specific to customer requirements can be offered

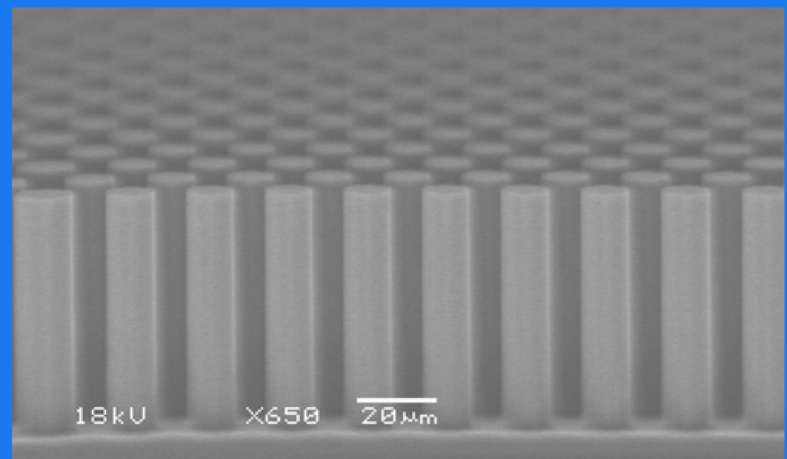
IceMOS offers a wide range of premium unit processing services for customers requiring high-quality fabrication on their own wafers.

We provide high-resolution Scanning Acoustic Microscope (SAM) imaging for our bonded BSOI and CSOI wafers, a service that is also available for customer-supplied bonded wafers.

SAM inspection is a non-destructive method for imaging bonded interfaces. Unlike conventional ultrasonic testing, infrared microscopy, or X-ray microscopy, SAM scans the specimen surface pixel-by-pixel and line-by-line using a specialized transducer to detect reflected ultrasonic waves. IceMOS SAM inspection features a detection limit of 10 µm for lateral delamination with a vertical resolution of 15 nm. We offer high-resolution whole-wafer scanning for diameters ranging from 100 mm to 200 mm, with pixel sizes as small as 20 µm; additionally, specific regions of interest can be scanned at even higher resolutions.

IceMOS Technology leverages deep engineering expertise to develop optimized process flows and CAD layouts, which are used to generate new mask sets or detailed cross-sectional concept drawings.

Our unit process foundry services maintain standards unsurpassed in the industry. With operations conducted within an IATF 16949 manufacturing environment—controlled by rigorous Statistical Process Control (SPC) and adhering to advanced CMOS contamination standards—IceMOS offers the ideal foundry solution. All services are supported by rapid turnaround times and a commitment to high on-time delivery compliance.

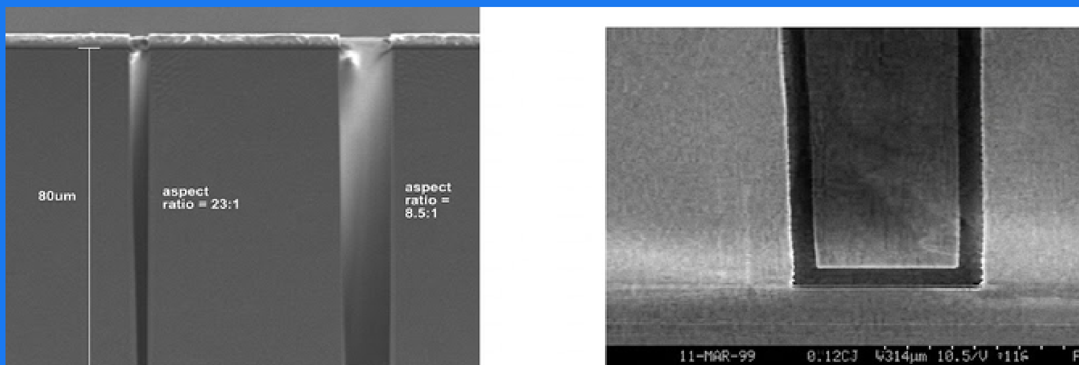


Example of IceMOS high density etch pillars.

Foundry Services

DRIE Etch Services

Deep trench etch is a core technology of IceMOS. With over 22 years' experience in this field, IceMOS Technology can offer DRIE Silicon etch options with minimum feature size 2um, on SOI up to 300um thick, trenches with aspect ratios of 20:1, large area patterns on SOI and Si wafers with exposed areas up to 65% and up to 500um through wafer etching on bulk Si and on SOI with aspect ratios up to 12:1. If required, our refill technology will not only ensure a completely filled trench, but will also leave a fully planar silicon surface for subsequent processing. Examples of just a small sample of what we can do are shown below. Contact our engineering team to discuss etch depth, sidewall angle, aspect ratio, exposed etch area and whether you require refill.



Neighbouring High and Low aspect ratio trenches in SOI without undercut.

Conformal Oxide & Poly refill in trenches etched in SOI.

Thin Film Depositions & Diffusion

Excellent process control and a suite of High temperature thermal oxidation and LPCVD TEOS oxide and LPCVD polysilicon allow IceMOS to offer excellent facilities for those wishing to refill etched features or deposit stacks of thermal or sacrificial oxide layers and heavily n++ doped or undoped LPCVD Polysilicon layers.

Process	Diameter	Min Thickness	Max Thickness	Tolerance (+/-)	Notes
Dry Oxidation	100mm, 125mm, 150mm & 200mm	24nm	200nm	15%	
Wet Oxidation	100mm, 125mm, 150mm & 200mm	100nm	6000nm	5%	
Undoped LPCVD Polysilicon	100mm, 125mm & 150mm	200nm	4500nm	10%	Per deposition
Heavily doped LPCVD Polysilicon (n++)	100mm, 125mm & 150mm	200nm	4500nm	10%	Per deposition
LPCVD TEOS	100mm, 125mm & 150mm	200nm	1000nm	5%	Densification at 1050C optional

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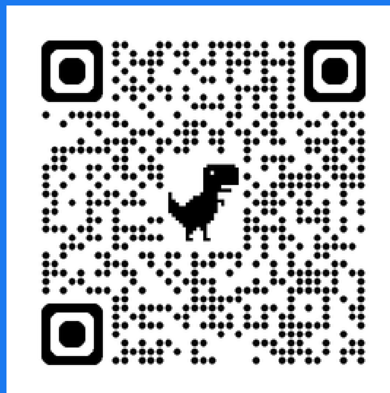

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