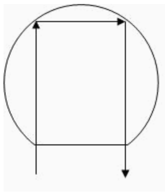
Part Number Customer

Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.30 mm	
	2.0	Primary Flat Orientation	{110}+/-1 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	None / Semi Standard	
	5.0	Overall Thickness	452.20 +/- 21.00 µm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00µm	Guaranteed by Process
	7.0	Bow	<60.00µm	ADE to ASTM F534, 20%
	8.0	Warp	<60.00µm	ADE to ASTM F657, 20%
	9.0	Edge Chips	0	Bright Light, 100%
	10.0	Edge Exclusion	6mm	
	11.0	LPDs > 0.3um	<=30	LPD particle count
HandleSilicon	12.0	Handle Growth Method	FZ	Wafer Vendor
	13.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	14.0	Handle Thickness	450.00 +/- 20.00 µm	ADE, 100%
	15.0	Handle Doping Type	N	Wafer Vendor
	16.0	Handle Dopant	Phosphorous	Wafer Vendor
	17.0	Handle Resistivity	>1000 Ohmcm	Wafer Vendor
	18.0	Backside Finish	Polished with oxide, laser mark, and light handling marks	Guaranteed by Process
BuriedOxide	19.0	Oxide Type	Thermal	
	20.0	Oxide Thickness	2,000.00 +/- 200.00 A	Nanospec centre point, 4%
	21.0	Oxide formed on	Handle and / or Device Wafer	
DeviceSilicon	22.0	Device Growth Method	FZ	Wafer Vendor
	23.0	Device Orientation	{100} +/- 1 degree	Wafer Vendor
	24.0	Nominal Thickness	2.00 +/- 0.50 µm	Filmetrics, 100% 9-Pt (note3)
	25.0	Distance to device silicon edge from wafer edge	<= 2.0mm	Typical by Process
	26.0	Device Doping Type	N	Wafer Vendor
	27.0	Device Dopant	Phosphorous	Wafer Vendor
	28.0	Device Resistivity	>1000 Ohmcm	Wafer Vendor
	29.0	Voids	none	Bright Light, 100% (note 2)
	30.0	Scratches	0	Bright Light, 100% (note 2)
	31.0	Haze	none	Bright Light, 100% (note 2)

Category	**Parameter**	**Specification**	**Measurement Method**
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	

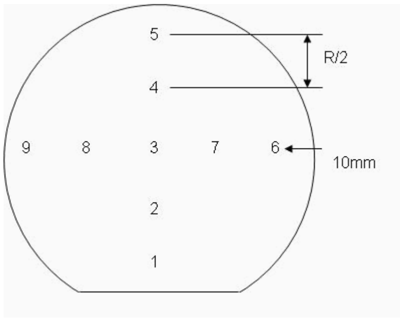
Explanatory Notes

1. Microscope inspection performed using microscope scan as below. 5x objective.



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information