

Part Number

Customer

Category	Parameter	Specification	Measurement Method	
OverallWafer	1.0	Diameter	150.00 +/- 0.20 mm	
	2.0	Primary Flat Orientation	{110} +/- 0.5 degree	Wafer Vendor
	3.0	Primary Flat Length	47.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none	
	5.0	Edge Rounding	Semi	Wafer Vendor
	6.0	Overall Thickness	627.00 +/- 5.00 μ m	ADE, 100%
	7.0	Total Thickness Variation (TTV)	<5.00 μ m	Guaranteed by Process
	8.0	Flatness (SBIR)	<1.00 μ m	20mm x 20mm, no partials, b/side ref, 100% UA
	9.0	Bow	<60.00 μ m	ADE to ASTM F534
	10.0	Warp	<60.00 μ m	ADE to ASTM F657
	11.0	Edge Chips	0	Bright Light, 100% (note 2)
	12.0	Edge Exclusion	3mm	
	13.0	Lasermarking	Back surface. Format: YYMM-XXXXX.5255A [Characters 11 to 16: .5255A]	Guaranteed by process
HandleSilicon	14.0	Handle Growth Method	CZ	Wafer Vendor
	15.0	Handle Oxygen Concentration	6.5e17 atcm-3 - 8.5e17 atcm-3 new ASTM	wafer vendor
	16.0	Handle Carbon Concentration	< 5e16 atcm-3 new ASTM	wafer vendor
	17.0	Handle Orientation	{100} +/- 1.0 degree	Wafer Vendor
	18.0	Handle Thickness	570.00 +/- 5.00 μ m	ADE, 100%
	19.0	Handle Doping Type	N	Wafer Vendor
	20.0	Handle Dopant	Phosphorous	Wafer Vendor
	21.0	Handle Resistivity	1.5 - 6.5 Ohmcm	Wafer Vendor
	22.0	Resistivity variation (within wafer)	RRV <20%. Within 6mm from edge. Semi Standard	Wafer Vendor
	23.0	Backside Finish	Lapped and Acid Etched with 2 μ m +/- 0.3 μ m oxide and lasermark .	Backside oxide not measured - guaranteed by process.
BuriedOxide	24.0	Oxide Type	Thermal	
	25.0	Oxide Thickness	20,000.00 +/- 1,000.00 A	Nanospec centre point, 4%
	26.0	Oxide formed on	Handle Wafer	
DeviceSilicon	27.0	Frontside surface finish	Mirror Polished	Guaranteed by process
	28.0	Device Growth Method	FZ	Wafer Vendor
	29.0	Oxygen Concentration	n/a	wafer vendor
	30.0	Carbon Concentration	< 2e16 atcm-3 new ASTM	wafer vendor
	31.0	Device Orientation	{100} +/- 0.5 degree	Wafer Vendor
	32.0	Nominal Thickness	55.00 +/- 1.00 μ m	Filmetrics, 100% 9-Pt (note3)

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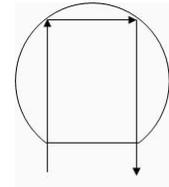
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DeviceSilicon	33.0	Distance to device silicon edge from wafer edge	<= 2mm	Typical by Process
	34.0	Device Doping Type	N	Wafer Vendor
	35.0	Device Dopant	Phosphorous	Wafer Vendor
	36.0	Device Resistivity	31.5 - 38.5 Ohm-cm	Wafer Vendor
	37.0	Buried Layer Implant	Species = As, Dose = 3e15, Energy = 100keV	Implant Vendor - 24nm screen oxide used
	38.0	Voids	none visible by bright light.	Bright Light, 100% (note 2)
	39.0	Scratches	none	Bright Light, 100% (note 2)
	40.0	Haze	none	Bright Light, 100% (note 2)
	41.0	Top surface particles	<= count 30 LPD, >= 0.3um. IceMOS Standard.	Tencor Particle Counter
	42.0	OISF	<= 10 cm-2. SEMI MF1727	Bright Light Inspection, 100%
	43.0	Other Surface Defects	Slip, Lineage, twin, shallow pits = None	Bright Light Inspection, 100%
	44.0	Dislocation Etch Pit Density	0 cm-2	Bright Light Inspection, 100%

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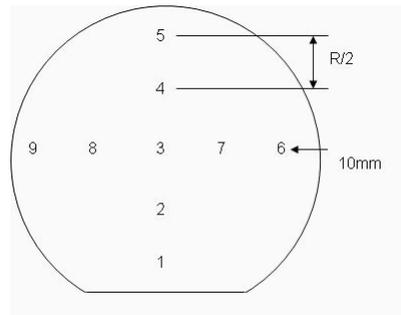
Shipping Details	Wafer per box :	Max 25
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness



Explanatory Notes 1. Microscope inspection performed using microscope scan as below. 5x objective.

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information