Part Number	Customer

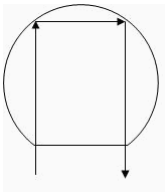
Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.20 mm	Wafer Vendor
	2.0	Primary Flat Orientation	{110}+/- 0.5 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	180deg to PFL +/- 5.0deg	Wafer Vendor
	5.0	Overall Thickness	514.00 +/- 11.00 µm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<3.00µm	Guaranteed by Process
	8.0	Bow	<80.00µm	ADE to ASTM F534, 20%
	9.0	Warp	<80.00µm	ADE to ASTM F657, 20%
	10.0	Edge Chips	0	Bright Light, 100% (note 2)
	11.0	Edge Exclusion	5mm	Guaranteed by process
	12.0	Lasermarking	Backside.	Guaranteed by process
HandleSilicon	14.0	Handle Growth Method	MCZ	Wafer Vendor
	15.0	Handle Orientation	{100} +/- 1.0 degree	Wafer Vendor
	16.0	Handle Doping Type	N	Wafer Vendor
	17.0	Handle Dopant	Phosphorus	Wafer Vendor
	18.0	Handle Resistivity	0.1 - 100 Ohm-cm	Wafer Vendor
	20.0	Handle Thickness	500.00 +/- 10.00 um	ADE, 100%
	21.0	Backside Finish	Polished with oxide, lasermarking and light handling marks. No Haze.	Guaranteed by Process and Visual Inspection.
BuriedOxide	22.0	Oxide Type	Thermal	Guaranteed by process
	23.0	Oxide Thickness	5,000.00 +/- 1,000.00 A	Nanospec centre point, 4%
	24.0	Oxide formed on	Handle (~250 nm) and Device Wafer (~250 nm)	Guaranteed by process
DeviceSilicon	31.0	Device Growth Method	MCZ	Wafer Vendor
	32.0	Device Orientation	{100} +/- 1.0 degree	Wafer Vendor
	33.0	Device Doping Type	N	Wafer Vendor
	34.0	Device Dopant	Phosphorus	Wafer Vendor
	35.0	Device Resistivity	5 - 10 Ohm-cm	Wafer Vendor
	36.0	Oxygen Concentration	6.0 ppma <= Oi <= 12.0 ppma	Wafer Vendor
	37.0	Nominal Thickness	13.00 +/- 0.50 um	FTIR, 100% 25-Pt (note3)
	38.0	Distance to device silicon edge from wafer edge	<= 2mm	Guaranteed by process
	39.0	Front Surface	Max 10 mm total length scratches, max 1 pit, No haze.	Bright Light inspection 100%
	40.0	Voids	none	Bright Light inspection 100%
	41.0	Scratches	Frontside- Max 10mm total length. Backside- Light handling marks allowed	Bright Light inspection 100%

Part Number	Customer

Category		Parameter	Specification	Measurement Method
DeviceSilicon	42.0	Haze	None: Frontside and Backside.	Bright Light inspection 100%
	43.0	SAM	Voids > 2.5 mm = NONE	SAM 100% inspection. Transfer SAM images to TDK for all wafers with CoC.
	44.0	Device Field Oxidation	1,000.00 +/- 100.00 A	Nanospec 5 points, 4% of wafers

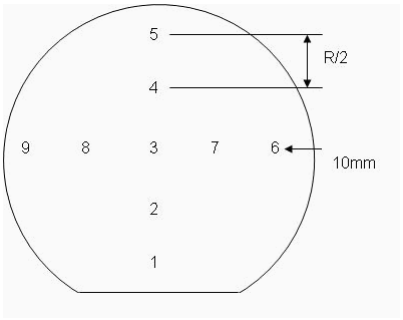
Part Number	Customer

Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	
Explanatory Notes	1. Microscope inspection performed using microscope scan as below. 5x objective.		



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information