Icemos Technology Ltd Product Specification 1000.759801 Issue Date 08 October 2024 17:1

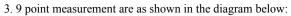
TO 1.37 1		
I Part Number	Customer	

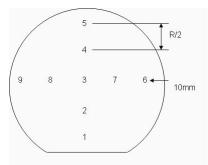
Category	Parameter		Specification	Measurement Method
OverallWafer	1.0	Diameter	150.00 +/- 0.50 mm	
	2.0	Primary Flat Orientation	{110}+/-1 degree	Wafer Vendor
	3.0	Primary Flat Length	57.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none	
	5.0	Overall Thickness	663.00 +/- 26.00 μm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00μm	Guaranteed by Process
	7.0	Bow	<60.00μm	ADE to ASTM F534, 20%
	8.0	Warp	<60.00μm	ADE to ASTM F657, 20%
	9.0	Edge Chips	0	Bright Light, 100%
	10.0	Edge Exclusion	5mm	
HandleSilicon	11.0	Handle Growth Method	CZ	Wafer Vendor
	12.0	Handle Orientation	{100}+/-1 degree	Wafer Vendor
	13.0	Handle Thickness	650.00 +/- 25.00 μm	ADE, 100%
	14.0	Handle Doping Type	N	Wafer Vendor
	15.0	Handle Dopant	Phos	Wafer Vendor
	16.0	Handle Resistivity	1~ 10 Ohmem	Wafer Vendor
	17.0	Backside Finish	Polished with lasermark and light handling marks	Wafer Vendor
DeviceSilicon	18.0	Device Growth Method	CZ	Wafer Vendor
	19.0	Device Orientation	{100}+/-1 degree	Wafer Vendor
	20.0	Nominal Thickness	13.00 +/- 1.00 μm	ADE single point 100%
	21.0	Distance to device silicon edge from wafer edge	<= 2 mm	Typical by Process
	22.0	Device Doping Type	N	Wafer Vendor
	23.0	Device Dopant	Phos or As	Wafer Vendor
	24.0	Device Resistivity	0.001-0.003 Ohm-cm	Wafer Vendor
	25.0	Voids	0	Bright Light, 100% (note 2)
	26.0	Scratches	total length < 5mm	Bright Light, 100% (note 2)
	27.0	Haze	none	Bright Light, 100% (note 2)

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Part Number		Customer		
Category	Parameter	Specification	Measurement Method	
Shipping Details	Wafer per box:	Max 25		
	Packaging:	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging		
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness		
Explanatory Notes	1. Microscope inspec	ction performed using microscope scan as below. 5x objective	e.	
	2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall			

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overal Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.





Additional Information