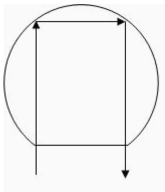
Part Number	Customer

Category		**Parameter**	**Specification**	**Measurement Method**
OverallWafer	1.0	Diameter	150.00 +/- 0.50 mm	
	2.0	Primary Flat Orientation	{110}+/-1 degree	Wafer Vendor
	3.0	Primary Flat Length	57.50 +/- 2.50 mm	Wafer Vendor
	4.0	OverallWafer Secondary Flat	None	
	5.0	Overall Thickness	1,009.00 +/- 27.80 µm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00µm	Guaranteed by Process
	7.0	Bow	<120.00µm	ADE to ASTM F534, 100%
	8.0	Warp	<120.00µm	
	9.0	Edge Chips	0	Bright Light, 100%
	10.0	Edge Exclusion	5mm	
	11.0	Lasermarking	On wafer BACKSIDE	Guaranteed by process
HandleSilicon	12.0	Handle Growth Method	CZ	Wafer Vendor
	13.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	14.0	Handle Thickness	525.00 +/- 25.00 µm	ADE, 100%
	15.0	Handle Doping Type	P	Wafer Vendor
	16.0	Handle Dopant	Boron	Wafer Vendor
	17.0	Handle Resistivity	>10 Ohmcm	Wafer Vendor
	18.0	Backside Finish	Polished with lasermark and oxide	Wafer Vendor
BuriedOxide	19.0	Oxide Type	Thermal	
	20.0	Oxide Thickness	40,000.00 +/- 8,000.00 A	Nanospec centre point, 4%
	21.0	Oxide formed on	Handle or/and Device	
DeviceSilicon	22.0	Device Growth Method	CZ	Wafer Vendor
	23.0	Device Orientation	{100} +/- 1 degree	Wafer Vendor
	24.0	Nominal Thickness	480.00 +/- 2.00 µm	Single Point ADE, 100%
	25.0	Distance to device silicon edge from wafer edge	<= 2mm	Typical by Process
	26.0	Device Doping Type	N or P	Wafer Vendor
	27.0	Device Dopant	Any	Wafer Vendor
	28.0	Device Resistivity	<0.01 Ohmcm	Wafer Vendor
	29.0	Voids	None by bright light inspection.	Bright Light, 100% (note 2)
	30.0	Scratches	0	Bright Light, 100% (note 2)
	31.0	Haze	None	Bright Light, 100% (note 2)

Category	**Parameter**	**Specification**	**Measurement Method**
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	

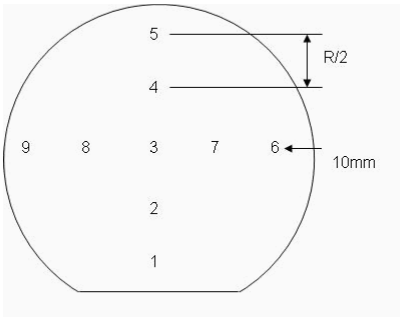
Explanatory Notes

1. Microscope inspection performed using microscope scan as below. 5x objective.



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information