

Part Number

Customer

Category	Parameter	Specification	Measurement Method	
OverallWafer	1.0	Diameter	100.00 +/- 0.50 mm	
	2.0	Primary Flat Orientation	{110} +/- 1.0 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none/semi standard	
	5.0	Secondary Flat Length	none / 18.5mm +/-2.5mm	Wafer Vendor
	6.0	Overall Thickness	702.00 +/- 26.00 μ m	ADE, 100%
	7.0	Total Thickness Variation (TTV)	<5.00 μ m	ADE 100%, SEMI MF1530.
	8.0	Bow	<60.00 μ m	ADE 100%, SEMI MF1390
	9.0	Warp	<60.00 μ m	ADE 100%, SEMI MF1390
	10.0	Edge Chips	0	Bright Light, 100%
	11.0	Edge Exclusion	5mm	
HandleSilicon	12.0	Handle Growth Method	Any	Wafer Vendor
	13.0	Handle Orientation	{100} +/- 1.0 degree	Wafer Vendor
	14.0	Handle Thickness	200.00 +/- 25.00 μ m	ADE, 100%
	15.0	Handle Doping Type	Intrinsic	Wafer Vendor
	16.0	Handle Dopant	None	Wafer Vendor
	17.0	Handle Resistivity	>10000 Ohm-cm	Wafer Vendor
	18.0	Backside Finish	Polished with oxide and lasermark.	Wafer Vendor
	BuriedOxide	19.0	Oxide Type	Thermal
20.0		Oxide Thickness	20,000.00 +/- 1,000.00 A	Nanospec centre point, 4%
21.0		Oxide formed on	Handle and / or device Wafer	
DeviceSilicon	22.0	Device Growth Method	Any	Wafer Vendor
	23.0	Device Orientation	{100} +/- 1.0 degree	Wafer Vendor
	24.0	Nominal Thickness	500.00 +/- 1.00 μ m	ADE, single point, 100%
	25.0	Distance to device silicon edge from wafer edge	<= 2mm	Typical by Process
	27.0	Device Doping Type	P	Wafer Vendor
	28.0	Device Dopant	Boron	Wafer Vendor
	29.0	Device Resistivity	<0.005 Ohm-cm	Wafer Vendor
	30.0	Voids	none	Wafer Vendor
	31.0	Scratches	0	Bright Light, 100% (note 2)
	32.0	Haze	none	Bright Light, 100% (note 2)

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Shipping Details	Wafer per box :	Max 25
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness



Explanatory Notes 1. Microscope inspection performed using microscope scan as below. 5x objective.

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information