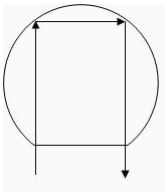
Part Number	Customer

Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.50 mm	
	2.0	Primary Flat Orientation	<110> +/- 0.5 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none / Semi Standard	
	5.0	Secondary Flat Length	none	Wafer Vendor
	6.0	Overall Thickness	502.00 +/- 12.00 µm	ADE 100%
	7.0	Total Thickness Variation (TTV)	<3.00µm	Guaranteed by Process
	8.0	Bow	<90.00µm	ADE to ASTM F534, 20%
	9.0	Warp	<90.00µm	ADE to ASTM F657, 20%
	10.0	Edge Chips	0	Bright Light, 100% (note 2)
	11.0	Edge Exclusion	5mm	
HandleSilicon	12.0	Handle Growth Method	CZ	Wafer Vendor
	13.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	14.0	Handle Thickness	400.00 +/- 10.00 µm	ADE, 100%
	15.0	Handle Doping Type	Any	Wafer Vendor
	16.0	Handle Dopant	P(Bor) / N(Ph)	Wafer Vendor
	17.0	Handle Resistivity	1 - 30 Ohmcm	Wafer Vendor
	19.0	Backside Finish	Polished with oxide and lasermark	Wafer Vendor
BuriedOxide	20.0	Oxide Type	Thermal	
	21.0	Oxide Thickness	20,000.00 +/- 2,000.00 A	Nanospec centre point, 4%
	22.0	Oxide formed on	Handle and Device Wafer	
DeviceSilicon	23.0	Device Growth Method	CZ	Wafer Vendor
	24.0	Device Orientation	{100} +/- 1 degree	Wafer Vendor
	25.0	Nominal Thickness	100.00 +/- 2.00 µm	FTIR, 100% 9-Pt (note3)
	26.0	Distance to device silicon edge from wafer edge	< 2 mm	Guaranteed by Process
	27.0	Device Doping Type	Any	Wafer Vendor
	28.0	Device Dopant	P(Bor) / N(Ph)	Wafer Vendor
	29.0	Device Resistivity	1- 30 Ohmcm	Wafer Vendor
	31.0	Voids	0	Bright Light, 100% (note 2)
	32.0	Scratches	0	Bright Light, 100% (note 2)
	33.0	Haze	none	Bright Light, 100% (note 2)

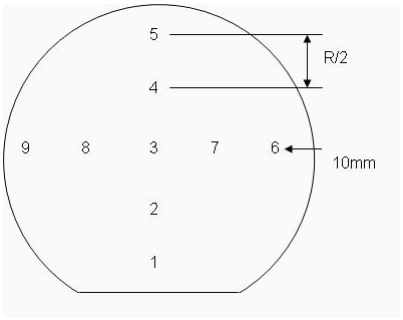
Part Number	Customer

Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	
Explanatory Notes	1. Microscope inspection performed using microscope scan as below. 5x objective.		



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information