Part Number	Customer

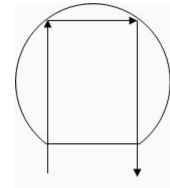
Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	150.00 +/- 0.30 mm	
	2.0	Notch or Flat	Notch	wafer vendor
	3.0	Notch Direction	{110} +/- 1 degree	wafer vendor
	4.0	Overall Thickness	676.00 +/- 6.10 µm	ADE, 100%
	5.0	Total Thickness Variation (TTV)	<5.00µm	Guaranteed by Process
	6.0	Bow	<60.00µm	ADE to ASTM F534, 20%
	7.0	Warp	<60.00µm	ADE to ASTM F657, 20%
	8.0	Edge Chips	0	Bright Light, 100% (note 2)
	9.0	Edge Exclusion	5mm	
HandleSilicon	10.0	Handle Growth Method	CZ	Wafer Vendor
	11.0	Handle Orientation	<100> +/- 1.0 degree	Wafer Vendor
	12.0	Handle Thickness	600.00 +/- 5.00 µm	ADE, 100%
	13.0	Handle Doping Type	P	Wafer Vendor
	14.0	Handle Dopant	Boron	Wafer Vendor
	15.0	Handle Resistivity	1 - 30 Ohmcm	Wafer Vendor
	16.0	Backside Finish	Polished with oxide and lasermarking and backside	Wafer Vendor
BuriedOxide	17.0	Oxide Type	Thermal	
	18.0	Oxide Thickness	10,000.00 +/- 500.00 A	Nanospec centre point, 4%
	19.0	Oxide formed on	Handle Wafer	
DeviceSilicon	20.0	Device Growth Method	CZ	Wafer Vendor
	21.0	Device Orientation	<100> +/- 1.0 degree	Wafer Vendor
	22.0	Nominal Thickness	75.00 +/- 1.00 µm	FTIR, 100% 9-Pt (note3)
	23.0	Distance to device silicon edge from wafer edge	< 2.0mm	Typical by Process
	24.0	Edge Removal Depth in Handle	<100um.	Guaranteed by process
	25.0	Device Doping Type	P	Wafer Vendor
	26.0	Device Dopant	Boron	Wafer Vendor
	27.0	Device Resistivity	0.01 - 0.025 Ohmcm	Wafer Vendor
	28.0	Voids	0	Bright Light, 100% (note2)
	29.0	Scratches	none	Bright Light, 100% (note2)
	30.0	Haze	none	Bright Light, 100% (note2)

Part Number	Customer

Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	

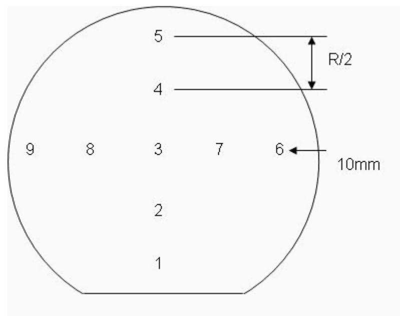
Explanatory Notes

1. Microscope inspection performed using microscope scan as below. 5x objective.



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information