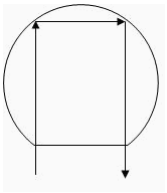
Part Number	Customer

Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	150.00 +/- 0.50 mm	Wafer vendor
	2.0	Primary Flat Orientation	{110}+/- 1.0 degree	Wafer vendor
	3.0	Primary Flat Length	57.50 +/- 2.50 mm	Wafer vendor
	4.0	Secondary Flat Orientation	None	Wafer vendor
	5.0	Overall Thickness	505.50 +/- 26.00 µm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00µm	Guaranteed by Process
	7.0	Bow	<60.00µm	ADE to ASTM F534,100%
	8.0	Warp	<60.00µm	ADE to ASTM F657, 100%
	9.0	Edge Chips	0	Bright Light, 100%
	10.0	Edge Exclusion	5mm	
HandleSilicon	11.0	Handle Growth Method	CZ	Wafer vendor
	12.0	Handle Orientation	{100} +/- 1 degree	Wafer vendor
	13.0	Handle Thickness	500.00 +/- 25.00 µm	ADE 100%
	14.0	Handle Doping Type	N	Wafer vendor
	15.0	Handle Dopant	Phos	Wafer vendor
	16.0	Handle Resistivity	<0.1 Ohm-cm	Wafer vendor
	17.0	Backside Finish	Polished with oxide and laser marking	Gurarranteed by process
BuriedOxide	18.0	Oxide Type	Thermal	Guaranteed by process
	19.0	Oxide Thickness	5,000.00 +/- 250.00 A	Nanospec centre point, 4%
	20.0	Oxide formed on	Device wafer	Guaranteed by process
DeviceSilicon	21.0	Device Growth Method	CZ	Wafer vendor
	22.0	Device Orientation	{100} +/- 1 degree	Wafer vendor
	23.0	Nominal Thickness	5.00 +/- 0.50 µm	Filmetrics 9 point, 100%
	24.0	Distance to device silicon edge from wafer edge	<= 2.0mm	Typical by process
	25.0	Device Doping Type	N	Wafer vendor
	26.0	Device Dopant	Phos	Wafer vendor
	27.0	Device Resistivity	10~25 Ohm-cm	Wafer vendor
	28.0	Voids	0	Bright Light, 100% (note 2)
	29.0	Scratches	0	Bright Light, 100% (note 2)
	30.0	Haze	none	Bright Light, 100% (note 2)

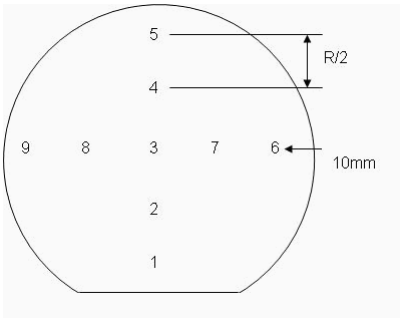
Part Number	Customer

Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	
Explanatory Notes	1. Microscope inspection performed using microscope scan as below. 5x objective.		



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information