Superior MEMS sensors from cavity silicon-on-insulator wafers

By Adele Gilliand, Applications Manager, IceMOS

Adele Gilliland, applications manager with IceMOS Technology Ltd. (Belfast, Northern Ireland), looks at how buried cavities in silicon can be used to enclose MEMS sensors and produce improved specifications.

Adele Gilliland, applications manager with IceMOS Technology Ltd.

Microelectromechanical systems (MEMS) design provides the basis for several different sensing technologies. According to one recent market forecast, the global MEMS sensors market was valued at USD 11,686.2 million in 2020 and is expected to reach USD 16,857.0 million by 2026, providing a compound annual growth rate (CAGR) of 6.5%. Pressure sensors are expected to experience the fastest growth rate due to their utilization in multiple application areas, such as biomedicine, automotive electronics, small home appliances, wearable, and fitness electronics. As pressure sensors become more widely used in the harsh environments found in industrial, automotive and aerospace applications, accurate high temperature pressure measurements become increasingly important.

MEMS Design

Several design and manufacturing approaches are used to combine the mechanical structures in the MEMS device to the signal conditioning and other circuitry that add functionality and value to the basic MEMS structure. The two most common approaches are MEMS first and MEMS last but there are variations between and within these two extremes.

With a MEMS-first approach, all the processing steps for the MEMS structure, including bulk micromachining, are performed prior to CMOS processing enabling the use of high temperatures that would damage or degrade CMOS. This means that temperatures greater than 1100°C can be used to obtain high-performance silicon on insulator substrates or release the stress in thick deposited polycrystalline silicon layers.

In contrast, a MEMS-last approach that typically uses surface micromachining to deposit and then etch layers or bulk micromachining for the mechanical structure must be kept below 400 or 450°C to avoid damaging the existing CMOS device. This means that high performance MEMS materials, such as monocrystalline and polycrystalline silicon, common in inertial sensors and resonators, cannot be used.

The advantages of MEMS-first design, together with the development of stable and CMOS-compatible wafer-level packaging solutions, enable flexible and cost-effective system on chip (SoC) solutions.

CSOI for High Temperature Use Cases

Sensors based on silicon-on-insulator (SOI) substrates have an advantage for MEMS devices produced for high-temperature applications because their structures provide greater flexibility in the micro-construction design and greater stability in the application.

Cavity silicon-on-insulator (CSOI) substrates have an even greater advantage over traditional SOI technology because the patterns are bonded facing inward resulting in buried cavities inside the wafer. The result is decreased parasitic capacitance between the device and handle layer of the SOI wafer, allowing for the device to function much more efficiently.

As a subset of SOI market, which is projected to grow from USD 1.0 billion in 2020 to USD 2.2 billion globally by 2025, at a CAGR of 15.7% from 2020 to 2025 according to a Market and Markets report, CSOI has equally attractive potential.

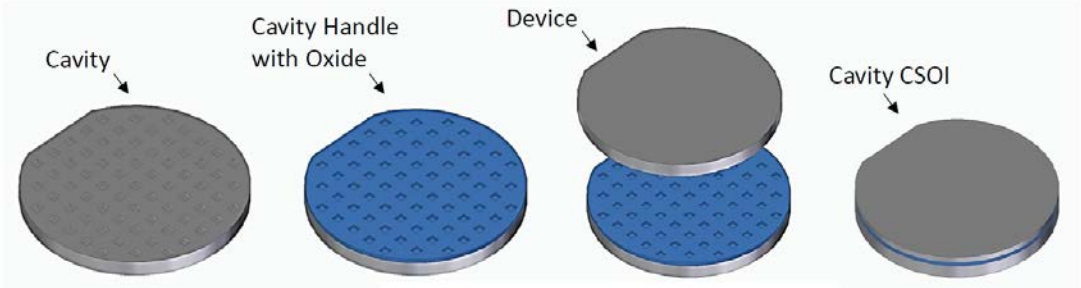
Because the bonding patterned wafer enables double-side processing of the SOI layer, CSOI also reduces device cost and size without compromising precision. By creating various structures within the cavity, including anchors, beams, pillars and more, developers of MEMS devices have increased design and manufacturing flexibility and it simplifies their silicon processing as well.

Bonding Technology for High Temperatures

Outsourcing the CSOI allows system designers to develop more intelligent devices by focusing on the value-added circuitry for the most demanding markets. Instead of simply purchasing starting wafers, these engineered silicon substrates enable a company to expand their MEMS sensor offering easily without making an investment into engineering or equipment resources. Fab managers can use their resources (equipment, time, and money) on processing device wafers for finished goods, not making substrates.

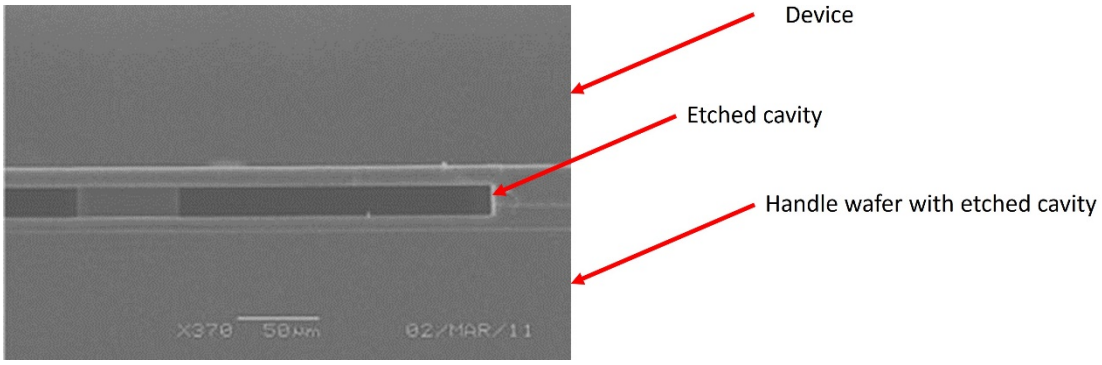
Substrate suppliers providing CSOI wafers need deep silicon trench etch expertise coupled with advanced wafer bonding technology to meet customer cavity requirements and create innovative products. Flexibility is also key. In addition to deep reactive ion etching (DRIE), other etching techniques can used depending on the desired structure and performance. There are various methods of constructing a CSOI wafer and advanced features can be incorporated, potentially opening possibilities that might otherwise not have been considered by the sensor developer.

In its basic form, IceMOS CSOI is two wafers with the cavity etched into one of the wafers and subsequently bonded to the other wafer, creating a vacuum. This process is especially good for sealed absolute pressure sensors because it provides a good quality reference and the cavity is hermetically sealed. As a result, it is the ideal advanced engineering substrate for manufacturing piezoresistive MEMS pressure sensors.



Caption: CSOI is two wafers with the cavity etched into one of the wafers and subsequently bonded to the other wafer, creating a vacuum.

The MEMS pressure sensor works on the principle of the deflection of a thin silicon membrane suspended over the cavity with changes in the environmental pressure relative to the fixed pressure within the bonded cavity. The mechanical deformation of the membrane can be converted into an electrical signal using piezoresistive, capacitive or optical detection techniques and the signal conversion and additional circuitry expertise of the sensor manufacturer.



Caption: Microphotograph cross-section of a CSOI engineering substrate.

Other more complex structures with multiple bonded silicon layers are available for advanced sensor design. CSOI substrates are the advanced starting wafer for inertial MEMS accelerometers, gyroscopes, and LiDAR sensors, in addition to other MEMS devices such as microphones, speakers, microfluidics, and resonators. With CSOI substrates, developers can make more efficient use of their engineering resources, better manage their MEMS fab capacity loading and cycle times, and, in many cases, reduce new product development and introduction time.

https://www.icemostech.com/

# # #