SiSi Solutions

Applications

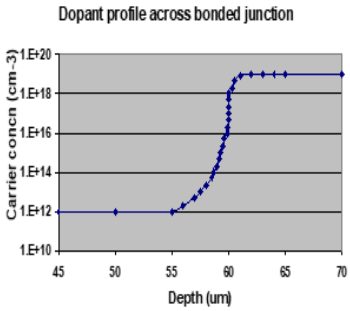
- High Voltage PIN Diodes
- RF Attenuators
- Photo Detectors
- X-Ray Detectors
- IR Sensors
- HV Power Devices
- Replacement for Epitaxial layers

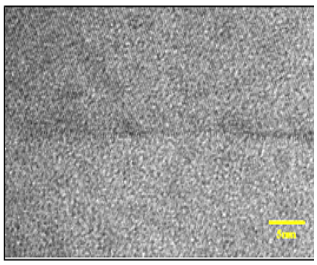
Key Features:

- High Quality
- Low cost
- Low defect density
- Excellent Layer uniformity
- Multiple layers
- Sharp transitions
- Layer resistivity up to 10kΩ-cm
- Excellent interface quality – verified by high resolution SAM Inspection

For semiconductor device manufacturers, the IceMOS Silicon – Silicon Direct bonded wafer offers a cost effective alternative to thick epitaxial layers and inverse epi that have traditionally been used for applications such as power devices and PiN diodes.

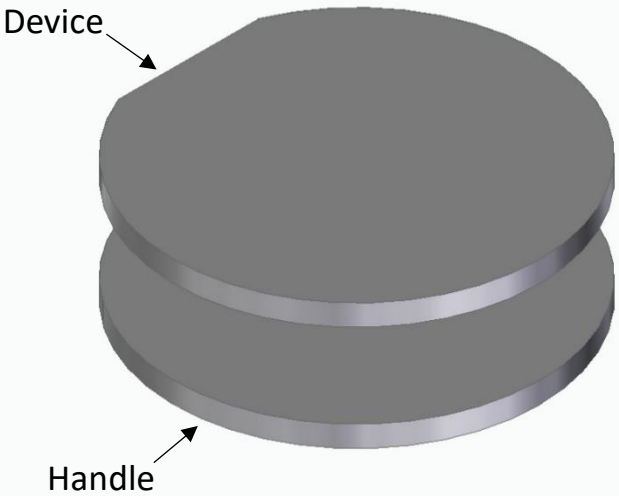
The use of direct wafer bonding technology allows silicon substrates to be produced containing multiple layers of single crystal silicon. These layers can have a resistivity range 1mΩ-cm to 10kΩ-cm, N and P-type and can include combinations of orientations – a feature not possible with conventional epitaxial wafers.

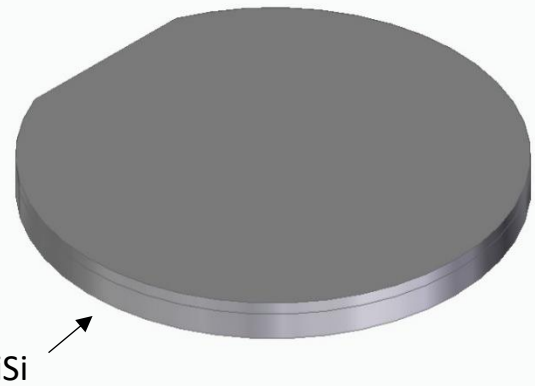




High resolution TEM image of SiSi wafer interface

The IceMOS SiSi bonding process gives a high quality wafer with low leakage, low warp and a low defect density. Additionally, the thickness variation in the layers can be as little as +/-0.5um. The transition between high and low dopant levels can be sharp or soft, depending on the application or customer requirement.





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"Cooler than Cool"™

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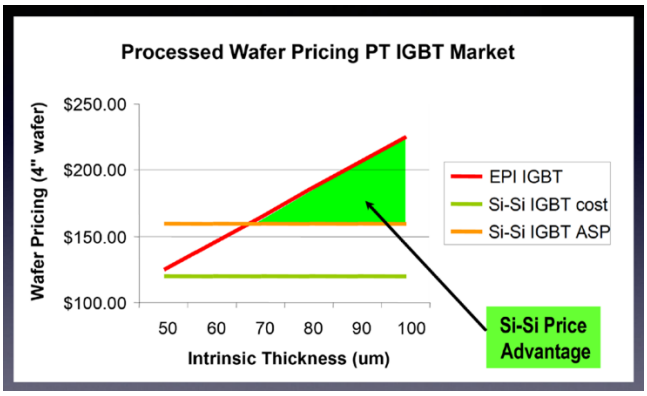

This chart shows the cost advantage of SiSi direct wafer bonding over Epi layers as a starting material for many electronic devices. This makes SiSi wafers an advantageous option for performance and cost reduction.

SiSi Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150 mm	200 mm
Handle Layer Specifications		
Handle Thickness	200–1100 µm	450–1100 µm
Handle Thickness Tolerance	±5 µm	
Stack Thickness	280–1150 µm	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω–cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Backside Finish	Lapped/Etched or Polished	
Device Layer Specifications		
Device Layer Thickness	≥20 µm	≥20 µm
Tolerance	± 0.5 µm	±0.8 µm
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω–cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Buried Layer Implant	N type or P type	

The above is a standard IceMOS specification; however, we are always happy to work with our customers to engineer specific solutions. If you would like to discuss an alternative specification, please contact our sales team: sales@icemostech.com

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