

Part Number

Customer

Category	Parameter	Specification	Measurement Method	
OverallWafer	1.0	Diameter	150.00 +/- 0.50 mm	
	2.0	Notch or Flat	NOTCH	
	3.0	Notch Direction	{110} +/- 1.0 degree	Wafer Vendor
	4.0	Overall Thickness	506.00 +/- 6.00 $\mu$ m	ADE, 100%
	5.0	Total Thickness Variation (TTV)	<5.00 $\mu$ m	Guaranteed by Process
	6.0	Bow	<80.00 $\mu$ m	ADE to ASTM F534, 100%
	7.0	Warp	<80.00 $\mu$ m	
	8.0	Edge Chips	0	Bright Light, 100% (note 2)
	9.0	Edge Exclusion	5mm	
HandleSilicon	10.0	Handle Growth Method	CZ	Wafer Vendor
	11.0	Handle Orientation	{100} +/- 0.5 degree	Wafer Vendor
	12.0	Handle Thickness	500.00 +/- 5.00 $\mu$ m	ADE, 100%
	13.0	Handle Doping Type	Any	Wafer Vendor
	14.0	Handle Dopant	Any	Wafer Vendor
	15.0	Handle Resistivity	> 1 Ohmcm	Wafer Vendor
	16.0	Backside Finish	Polished with light handling marks, Oxide and lasermark	Wafer Vendor
BuriedOxide	17.0	Oxide Type	Thermal	
	18.0	Oxide Thickness	10,000.00 +/- 500.00 A	Nanospec centre point, 4%
DeviceSilicon	19.0	Device Growth Method	CZ	Wafer Vendor
	20.0	Device Orientation	{100} +/- 0.5 degree	Wafer Vendor
	21.0	Nominal Thickness	5.00 +/- 0.50 $\mu$ m	Filmetrics, 9 point, 100%
	22.0	Distance to device silicon edge from wafer edge	<= 2mm	Typical by Process
	23.0	Edge Removal Depth in Handle	<100 $\mu$ m	Guaranteed by process
	24.0	Device Doping Type	Any	Wafer Vendor
	25.0	Device Dopant	Any	Wafer Vendor
	26.0	Device Resistivity	>3 Ohmcm	Wafer Vendor
	27.0	Voids	none	Bright Light, 100% (note 2)
	28.0	Scratches	0	Bright Light, 100% (note 2)
29.0	Haze	none	Bright Light, 100% (note 2)	
	30.0	Device Field Oxidation	0.00 +/- 0.00 A	Thickness TBC - Nanospec centre point, 4%

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Shipping Details	Wafer per box :	Max 25
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness



Explanatory Notes 1. Microscope inspection performed using microscope scan as below. 5x objective.

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information