

## ICE20N60FP N-Channel Enhancement Mode MOSFET

RoHS compliant  
2011/65/EU

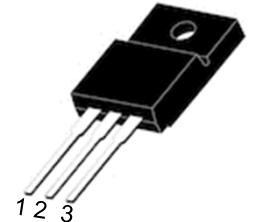
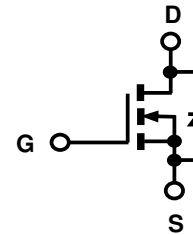


HALOGEN  
FREE

Product Summary			
$I_D$	$T_A=25^\circ\text{C}$	20A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	600V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.17 $\Omega$	Typ
$Q_g$	$V_{DS}=480\text{V}$	59nC	Typ

### Features

- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



T0220FP

Isolated (T0-220)

1=Gate, 2=Drain,  
3=Source.

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

**Maximum ratings**<sup>b</sup> at  $T_j=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_c=25^\circ\text{C}$	20	A
		$T_c=100^\circ\text{C}$	11	
Pulsed drain current	$I_{D, pulse}$	$T_c=25^\circ\text{C}$	62	A
Avalanche energy, single pulse	$E_{AS}$	$I_D=10\text{A}$	520	mJ
Avalanche current, repetitive	$I_{AR}$	limited by $T_{j,max}$	10	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=480\text{V}$ , $I_D=20\text{A}$ , $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	$V_{GS}$	Static	$\pm 20$	V
		AC ( $f>1\text{Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_c=25^\circ\text{C}$	35	W
Operating and storage temperature	$T_j$ , $T_{stg}$		-55 to +150	$^\circ\text{C}$
Mounting torque		M 3 & 3.5 screws	50	Ncm

a When mounted on 1inch square 2oz copper clad FR-4

b limited by  $T_{j,max}$

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

### Thermal characteristics

Thermal resistance, junction-case <sup>a</sup>	$R_{thJC}$		-	-	3.5	°C/W
Thermal resistance, junction-ambient <sup>a</sup>	$R_{thJA}$	leaded	-	-	72	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

### Electrical characteristics at $T_j=25^{\circ}\text{C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	600	650	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3.0	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=150^{\circ}\text{C}$	-	100	-	
Gate source leakage current	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=10\text{A}, T_j=25^{\circ}\text{C}$	-	0.17	0.19	$\Omega$
		$V_{GS}=10\text{V}, I_D=10\text{A}, T_j=150^{\circ}\text{C}$	-	0.49	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	3.8	-	$\Omega$

#### Dynamic characteristics

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, f=1\text{ MHz}$	$V_{DS}=25\text{ V}$	-	2064	-	pF
Output capacitance	$C_{oss}$		$V_{DS}=100\text{ V}$	-	87	-	
Reverse transfer capacitance	$C_{rss}$		$V_{DS}=25\text{ V}$	-	18	-	
Transconductance	$g_{fs}$	$V_{DS}>2 * I_D * R_{DS}, I_D=10\text{A}$		-	17	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{V}, V_{GS}=10\text{V}, I_D=20\text{A}, R_G=4\Omega \text{ (External)}$		-	148	-	ns
Rise time	$t_r$			-	40	-	
Turn-off delay time	$t_{d(off)}$			-	129	-	
Fall time	$t_f$			-	23	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

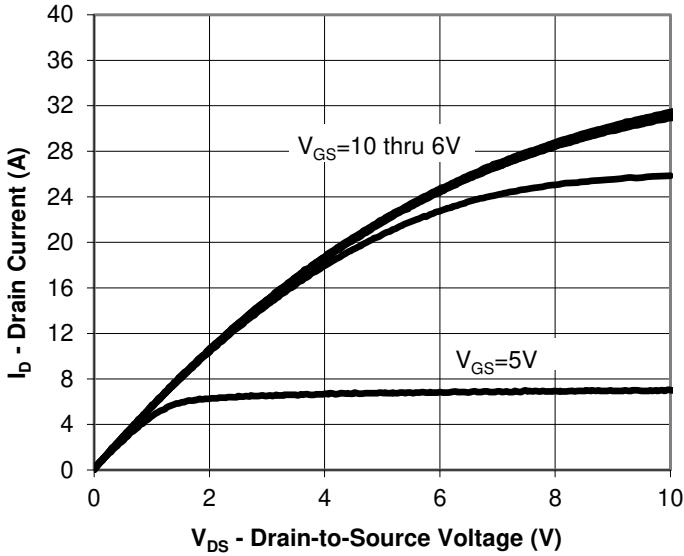
### Gate charge characteristics

Gate to source charge	$Q_{gs}$	$V_{DS}=480\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	8	-	nC
Gate to drain charge	$Q_{gd}$		-	19	-	
Gate charge total	$Q_g$		-	59	-	
Gate plateau voltage	$V_{plateau}$		-	4.2	-	V

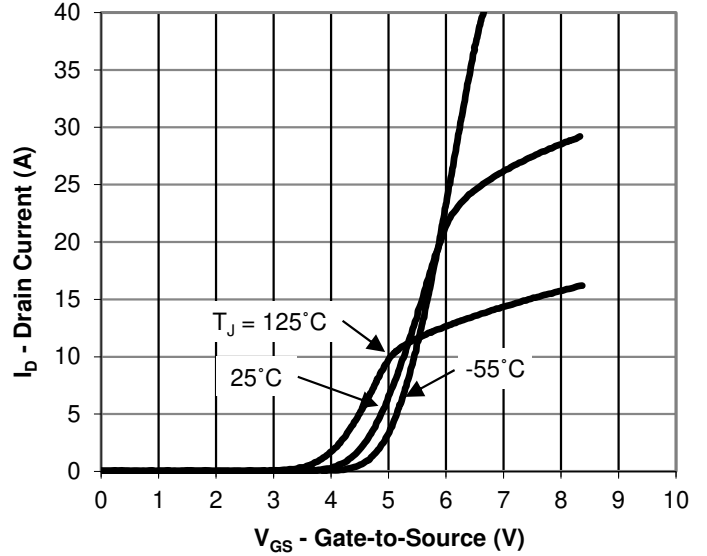
### Reverse Diode

Continuous forward current	$I_S$	$V_{GS}=0\text{ V}$	-	-	20	A
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_S=I_F$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$V_{RR}=480\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	358	-	ns
Reverse recovery charge	$Q_{rr}$		-	6.8	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rm}$		-	43.1	-	A

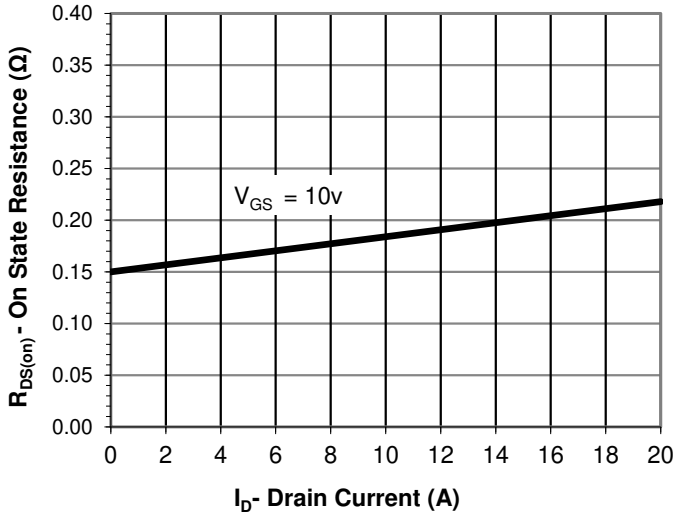
**Output Characteristics**



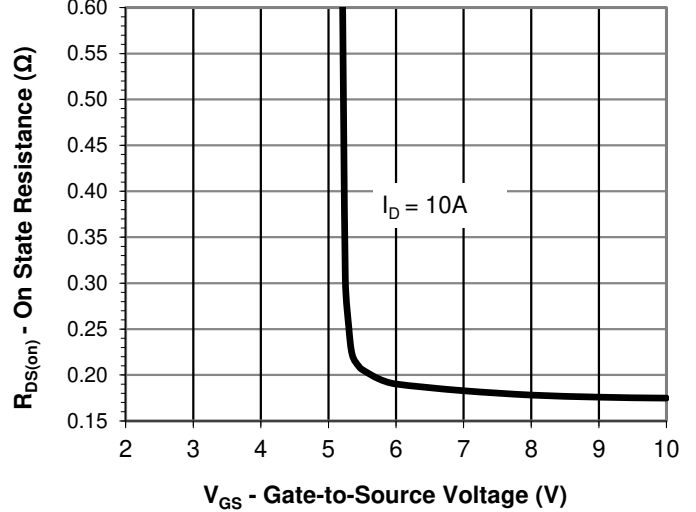
**Transfer Characteristics**



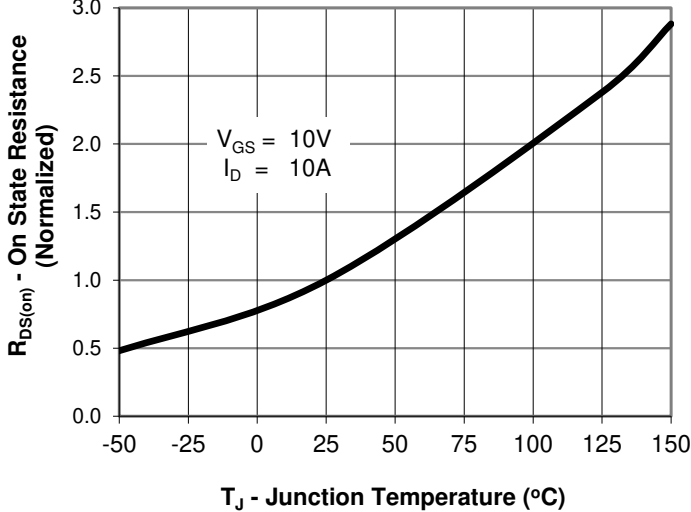
**Drain-Source On-State Resistance vs. Drain Current**



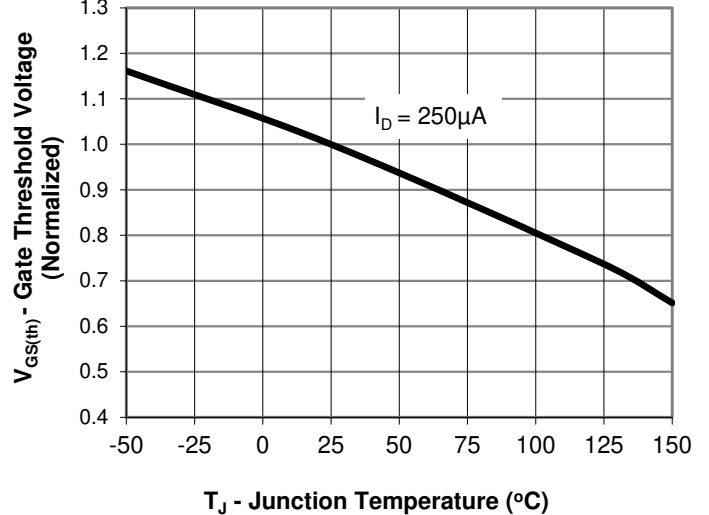
**Drain-Source On-State Resistance vs. Gate-to-Source Voltage**



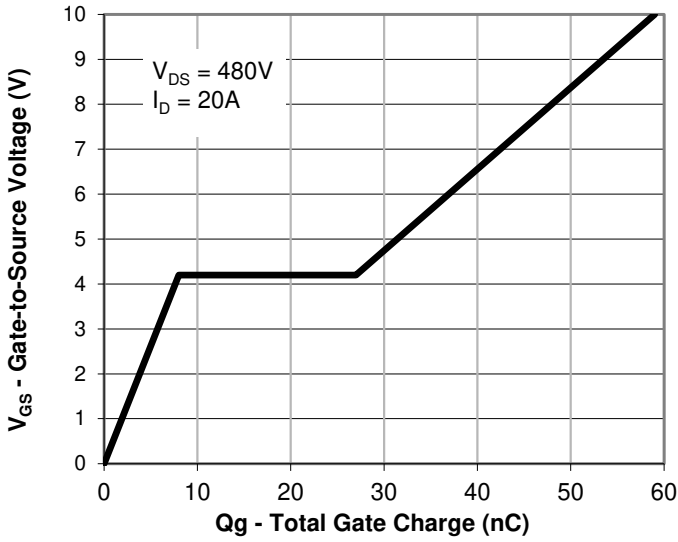
**Drain-Source On State Resistance vs. Junction Temperature**



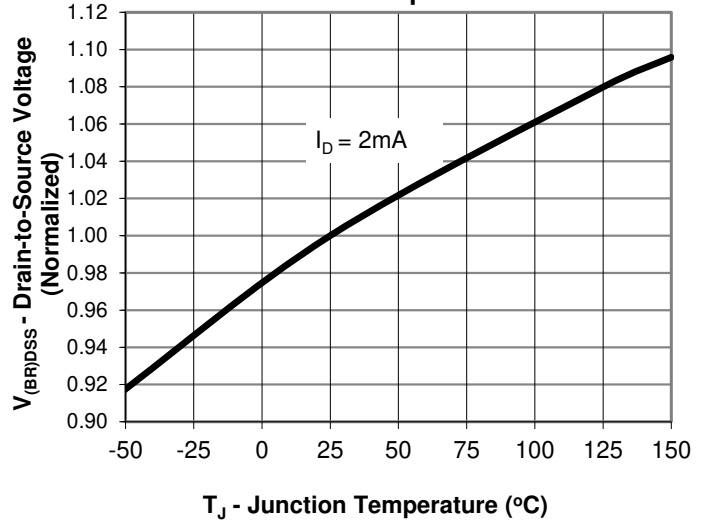
**Gate Threshold Voltage vs. Junction Temperature**



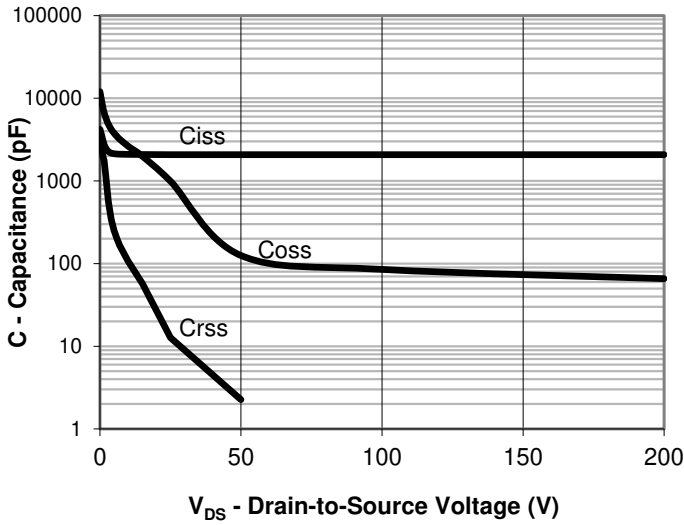
**Gate Charge**



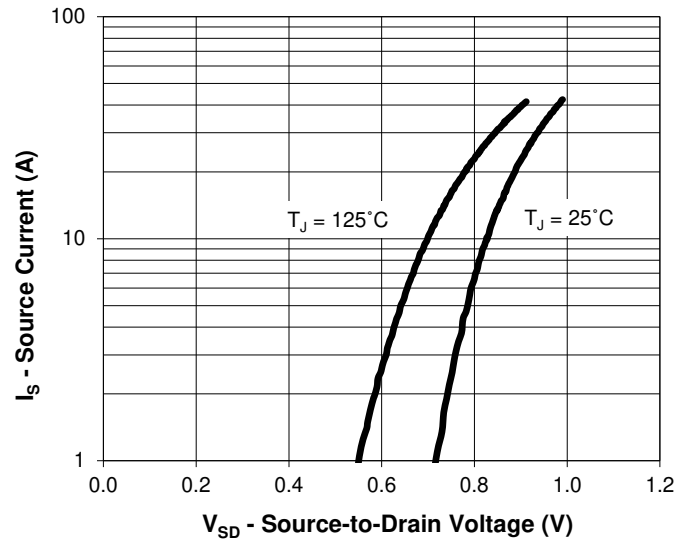
**Drain-to-Source Breakdown Voltage vs. Junction Temperature**



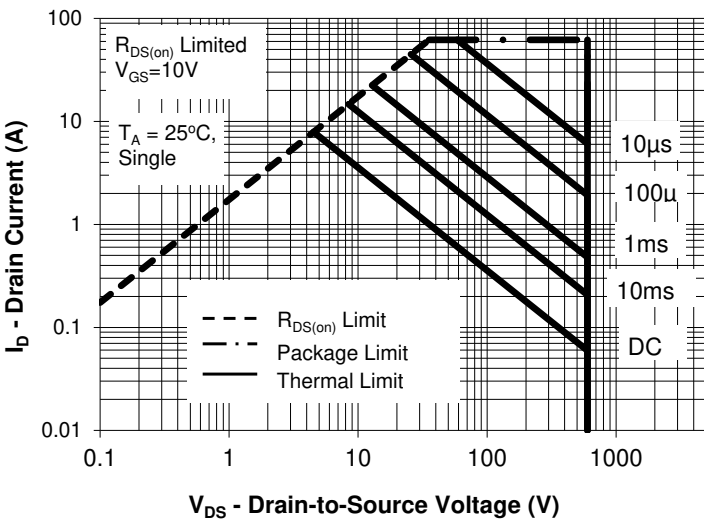
**Capacitance**



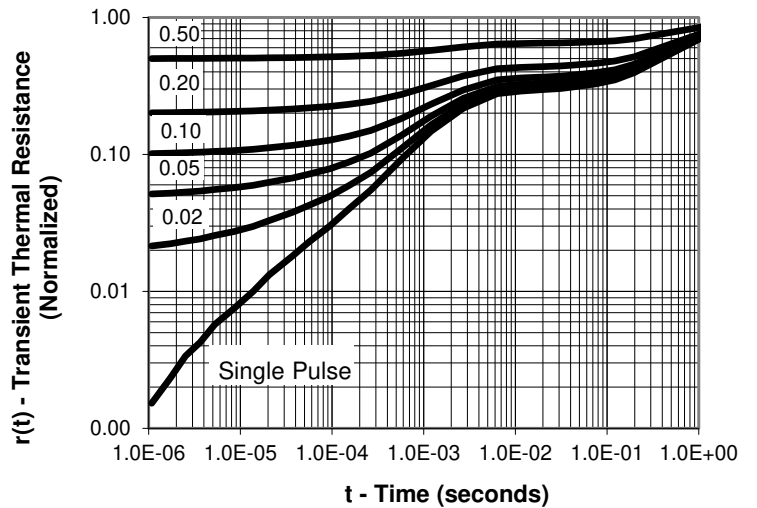
**Source-Drain Diode Forward Voltage**



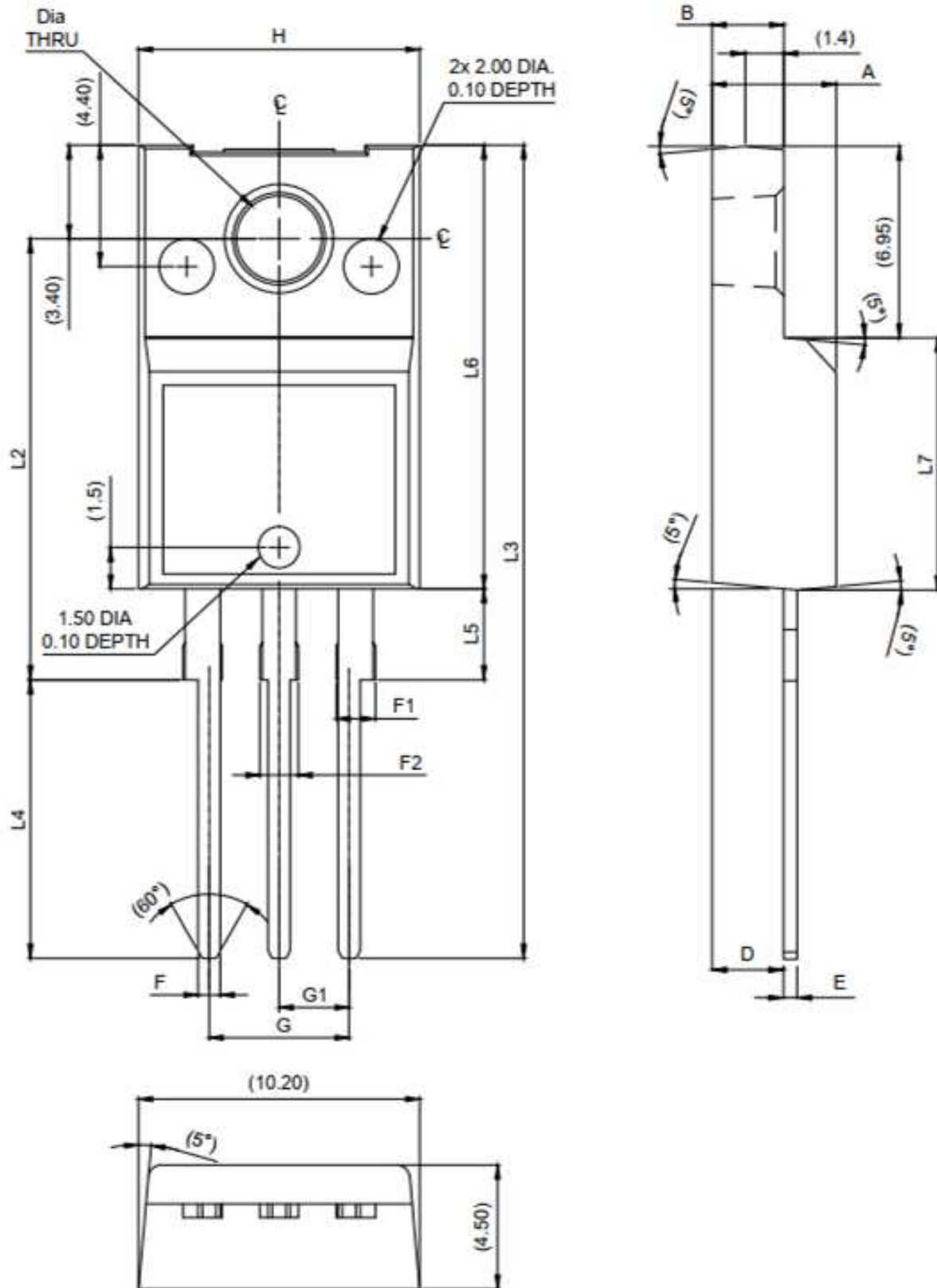
**Full Pak TO-220 Package  
Maximum Rated Forward Biased SOA**



**Full Pak TO-220 Transient Thermal Response, Junction-to-Ambient**



Package Outline: TO-220 FullPAK



## Package Outline: TO-220 FullPAK

SYMBOL	MIN	NOM	MAX	NOTES
A	4.4		4.6	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994. 2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
B	2.5		2.7	
D	2.5		2.75	
E	0.45		0.7	
F	0.75		1	
F1	1.15		1.5	
F2	1.15		1.5	
G	4.95		5.2	
G1	2.4		2.7	
H	10		10.4	
L2		16		
L3	28.6		30.6	
L4	9.8		10.6	
L5	2.9		3.6	
L6	15.9		16.4	
L7	9		9.3	
Dia	3		3.2	

# ICEMOS SUPERJUNCTION PATENT PORTFOLIO

## ICEMOS GRANTED PATENTS

US7,429,772

US7,439,178

US7,446,018

US7,579,607

US7,723,172

US7,795,045

US7,846,821

US7,944,018

US8,012,806

US8,030,133

## 3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2

US7,023,069B2

US7,364,994

US7,227,197B2

US7,304,944B2

US7,052,982B2

US7,339,252

US7,410,891

US7,439,583

US7,227,197B2

US6,635,906

US6,936,867

US7,015,104

US9,109,110

US7,271,067

US7,354,818

US7,052,982,

US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.



## Marking Information

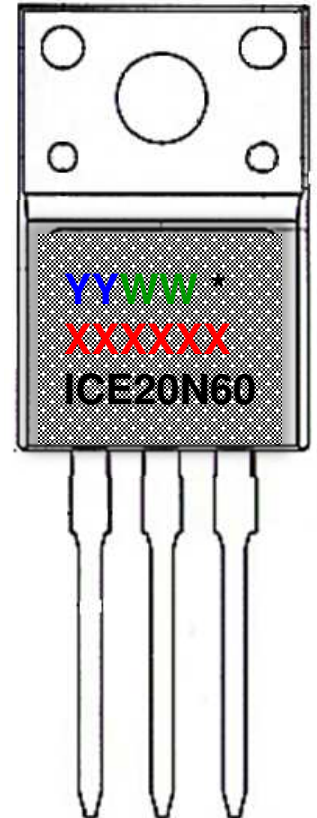
**YY** = Last two digits of the year

**WW** = Work week calendar on Icemos subcon assembly & test house

**\*** = Site ID

**XXXXXX** = Lot ID

**ICE20N60** = ICE is IceMOS logo and 20N60 is a designated device part number



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