Icemos Technology Ltd Product Specification 1000.531702 Issue Date 13 June 2018 16:28:58

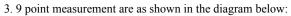
D M 1	O 4	
Part Number	Customer	

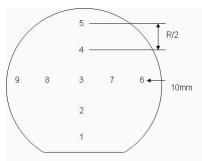
Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	150.00 +/- 0.20 mm	
	2.0	Primary Flat Length	57.50 +/- 2.50	Wafer Vendor
	3.0	Primary Flat Orientation	<110> +/- 1 degree	Wafer Vendor
	4.0	Overall Thickness	559.50 +/- 16.00 μm	ADE, 100%
	5.0	Total Thickness Variation (TTV)	<5.00μm	Guaranteed by Process
	6.0	Bow	<80.00μm	ADE to ASTM F534, 20%
	7.0	Warp	<80.00μm	ADE to ASTM F657, 20%
	8.0	Edge Chips	0	Bright Light, 100% (note 2)
	9.0	Edge Exclusion	5mm	
HandleSilicon	10.0	Handle Growth Method	CZ	Wafer Vendor
	11.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	12.0	Handle Thickness	550.00 +/- 15.00 μm	ADE, 100%
	13.0	Handle Doping Type	P	Wafer Vendor
	14.0	Handle Dopant	Boron	Wafer Vendor
	15.0	Handle Resistivity	1 - 30 Ohmem	Wafer Vendor
	16.0	Backside Finish	Lapped and etched with no oxide	Wafer Vendor
BuriedOxide	17.0	Oxide Type	Thermal	
	18.0	Oxide Thickness	5,000.00 +/- 250.00 A	Nanospec centre point, 4%
	19.0	Oxide formed on	Handle Wafer	
DeviceSilicon	20.0	Device Growth Method	CZ	Wafer Vendor
	21.0	Device Orientation	{100} +/- 1 degree	Wafer Vendor
	22.0	Nominal Thickness	9.00 +/- 1.00 μm	FTIR, 100% 9-Pt (note3)
	23.0	Distance to device silicon edge from wafer edge	<= 2 mm	Typical by Process
	24.0	Device Doping Type	P	Wafer Vendor
	25.0	Device Dopant	Boron	Wafer Vendor
	26.0	Device Resistivity	1 - 30 Ohm-cm	Wafer Vendor
	27.0	Voids	0	Bright Light, 100% (note 2)
	28.0	Scratches	none	Bright Light, 100% (note 2)
	29.0	Haze	none	Bright Light, 100% (note 2)

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Part Number		Customer		
Category	Parameter	Specification	Measurement Method	
Shipping Details	Wafer per box :	Max 25		
	Packaging:	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging		
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness		
Explanatory Notes	1. Microscope inspec	tion performed using microscope scan as below. 5x objective.		
	2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall			

Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.





Additional Information