Icemos Technology Ltd Product Specification 1000.522202 Issue Date 23 October 2019 16:1

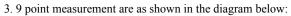
Part Number	Customer

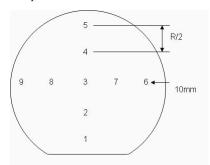
Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.20 mm	
	2.0	Primary Flat Orientation	{110}+/-1 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none/semi	
	5.0	Overall Thickness	551.00 +/- 15.00 μm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00μm	Guaranteed by Process
	7.0	Bow	<80.00μm	ADE to ASTM F534, 20%
	8.0	Warp	<80.00μm	ADE to ASTM F657, 20%
	9.0	Edge Chips	0	Bright Light, 100% (note 2)
	10.0	Edge Exclusion	5mm	
HandleSilicon	11.0	Handle Growth Method	FZ	Wafer Vendor
	12.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	13.0	Handle Thickness	225.00 +/- 10.00 μm	ADE, 100%
	14.0	Handle Doping Type	Any	Wafer Vendor
	15.0	Handle Dopant	Any	Wafer Vendor
	16.0	Handle Resistivity	>2000 Ohm cm	Wafer Vendor
	17.0	Backside Finish	Polished with oxide and lasermarking	Guaranteed by Process
BuriedOxide	18.0	Oxide Type	Thermal	
	19.0	Oxide Thickness	10,000.00 +/- 500.00 A	Nanospec centre point, 4%
	20.0	Oxide formed on	Handle Wafer	
DeviceSilicon	21.0	Device Growth Method	FZ	Wafer Vendor
	22.0	Device Orientation	{100} +/- 1 degree	Wafer Vendor
	23.0	Nominal Thickness	325.00 +/- 2.00 μm	ADE Single point, 100%
	24.0	Device Doping Type	Any	Wafer Vendor
	25.0	Device Dopant	Any	Wafer Vendor
	26.0	Device Resistivity	>2000 Ohmem	Wafer Vendor
	27.0	Voids	none	Wafer Vendor
	28.0	Scratches	0	Bright Light, 100% (note 2)
	29.0	Haze	none	Bright Light, 100% (note 2)

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Part Number		Customer	
Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box:	Max 25	
	Packaging:	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	
Explanatory Notes	1. Microscope inspec	tion performed using microscope scan as below. 5x objective.	
		pections performed exclude all wafer area outside the edge exclusion	on defined in Overall

Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.





Additional Information