Icemos Technology Ltd Product Specification 1000.312102 Issue Date 21 February 2017 16::

Part Number (	7
Part Number (	Customer

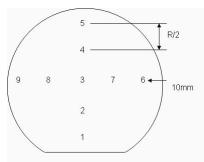
Category	Parameter		Specification	Measurement Method
OverallWafer	1.0	Silicon Supplier	Topsil Global Wafers	Wafer Vendor
	2.0	Diameter	100.00 +/- 0.50 mm	WaferVendor
	3.0	Primary Flat Orientation	<110> +/- 1 degree	Wafer Vendor
	4.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	5.0	Secondary Flat Orientation	none	Wafer Vendor
	6.0	Overall Thickness	970.00 +/- 7.00 um	Guaranteed by Process
	7.0	Total Thickness Variation (TTV)	<5.00um	Guaranteed by Process
	8.0	Bow	<40.00um	Guaranteed by Process
	9.0	Warp	<40.00um	Guaranteed by Process
	10.0	Edge Exclusion	5 mm	Guaranteed by Process
HandleSilicon	11.0	Handle Growth Method	CZ	Wafer Vendor
	12.0	Handle Orientation	<111> off 2.5 - 3.5deg	Wafer Vendor
	13.0	Handle Thickness	670.00 +/- 5.00 um	Guaranteed by Process
	14.0	Handle Doping Type	P	Wafer Vendor
	15.0	Handle Dopant	Boron	Wafer Vendor
	16.0	Handle Resistivity	< 0.005	Wafer Vendor
	17.0	Backside Finish	Lapped and etched with no oxide and lasermark	Wafer Vendor
DeviceSilicon	18.0	Device Growth Method	FZ	Wafer Vendor
	19.0	Device Orientation	<111> +/- 1 degree	Wafer Vendor
	20.0	Nominal Thickness	300.00 +/- 2.00 um	Guaranteed by Process, ADE single point, 100%
	21.0	Distance to device silicon edge from wafer edge	<= 2mm	Guaranteed by Process
	22.0	Device Doping Type	P	Guaranteed by Process
	23.0	Device Dopant	Boron	Guaranteed by Process
	24.0	Device Resistivity	12000 - 20000 Ohmem	Wafer Vendor
	25.0	Voids	none	Guaranteed by Process, SAM inspection
	26.0	Haze	none	Guaranteed by Process, Bright LIght inspection
	27.0	Scratches	none	Guaranteed by Process, Bright LIght inspection

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Category	Parameter	Specification	Measurement Method
Shipping Details	Wafer per box :	Max 25	
	Packaging:	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	
Explanatory Notes	1. Microscope inspec	ction performed using microscope scan as below. 5x objective.	
	2. All bright light ins	spections performed exclude all wafer area outside the edge exclusion	on defined in Overall

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overal Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information