

Part Number

Customer

Category	Parameter	Specification	Measurement Method	
OverallWafer	1.0	Diameter	150.00 +/- 0.20 mm	
	2.0	Primary Flat Orientation	{110} +/- 0.5 degree	Wafer Vendor
	3.0	Primary Flat Length	57.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none	
	5.0	Overall Thickness	677.00 +/- 25.00 μ m	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00 μ m	Guaranteed by Process
	7.0	Bow	<60.00 μ m	ADE to ASTM F534, 20%
	8.0	Warp	<60.00 μ m	ADE to ASTM F657, 20%
	9.0	Edge Chips	0	Bright Light, 100% (note 2)
	10.0	Edge Exclusion	3mm	
HandleSilicon	11.0	Handle Growth Method	CZ	Wafer Vendor
	12.0	Handle Orientation	{100} +/- 0.5 degree	Wafer Vendor
	13.0	Handle Thickness	555.00 +/- 25.00 μ m	ADE, 100%
	14.0	Handle Doping Type	N	Wafer Vendor
	15.0	Handle Dopant	Phosphorous	Wafer Vendor
	16.0	Handle Resistivity	1 - 50 Ohmcm	Wafer Vendor
	17.0	Backside Finish	Polished with no oxide and no lasermark	Wafer Vendor
BuriedOxide	18.0	Oxide Type	Thermal	
	19.0	Oxide Thickness	20,000.00 +/- 1,000.00 A	Nanospec centre point, 4%
	19.5	Oxide formed on	Handle Wafer	
DeviceSilicon	20.0	Device Growth Method	CZ	Wafer Vendor
	21.0	Device Orientation	{100} +/- 0.5 degree	Wafer Vendor
	22.0	Nominal Thickness	120.00 +/- 1.00 μ m	FTIR, 100% 9-Pt (note3)
	23.0	Distance to device silicon edge from wafer edge	<= 1.5mm	Defined
	24.0	Device Doping Type	N	Wafer Vendor
	25.0	Device Dopant	Phosphorous	Wafer Vendor
	26.0	Device Resistivity	1 - 10 Ohm-cm	Wafer Vendor
	26.5	Buried Layer Implant	none	implant vendor
	28.0	Voids	0	Bright Light, 100% (note 2)
	29.0	Scratches	0	Bright Light, 100% (note 2)
30.0	Haze	none	Bright Light, 100% (note 2)	

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Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	



Explanatory Notes 1. Microscope inspection performed using microscope scan as below. 5x objective.

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information