

Part Number

Customer

Category	Parameter	Specification	Measurement Method	
OverallWafer	1.0	Diameter	150.00 +/- 0.50 mm	Wafer Vendor
	2.0	Primary Flat Orientation	{110} +/- 0.5 degree	Wafer Vendor
	3.0	Primary Flat Length	57.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	none	
	5.0	Overall Thickness	562.00 +/- 26.00 μm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00μm	Guaranteed by Process
	7.0	Bow	<80.00μm	ADE to ASTM F534, 20%
	8.0	Warp	<80.00μm	ADE to ASTM F657, 20%
	9.0	Edge Chips	0	Bright Light, 100% (note 2)
	10.0	Edge Exclusion	5mm	
HandleSilicon	11.0	Handle Growth Method	CZ	Wafer Vendor
	12.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	13.0	Handle Doping Type	ANY	Wafer Vendor
	14.0	Handle Dopant	ANY	Wafer Vendor
	15.0	Handle Resistivity	>0.01 Ohmcm	Wafer Vendor
	16.0	Handle Thickness	550.00 +/- 20.00 um	ADE, 100%
	17.0	Backside Finish	Lapped with oxide and laser marking	Guaranteed by process
BuriedOxide	18.0	Oxide Type	Thermal	Guaranteed by process
	19.0	Oxide Thickness Handle	10,000.00 +/- 500.00 A	Nanospec
DeviceSilicon	20.0	Device Growth Method	CZ	Formed using SOI Layer Transfer
	21.0	Device Orientation	{100} +/- 0.5 degree	Wafer Vendor
	22.0	Device Doping Type	N	Wafer Vendor
	23.0	Device Dopant	Phosphorous	Wafer Vendor
	24.0	Device Resistivity	0.5 - 3 Ohmcm	Wafer Vendor
	25.0	Nominal Thickness	10.00 +/- 0.80 um	Post Field oxidation 9 point measurement
	26.0	Distance to device silicon edge from wafer edge	<2mm	Guaranteed by process
	27.0	Voids	none inside 5mm edge exclusion	Bright Light inspection 100%
	28.0	Scratches	none	Bright Light inspection 100%
	29.0	Haze	none	Bright Light inspection
30.0	Device Field Oxidation	10,000.00 +/- 500.00 um	Nanospec	

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Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 150.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	



Explanatory Notes 1. Microscope inspection performed using microscope scan as below. 5x objective.

2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information