Icemos Technology Ltd Product Specification 1000.455101 Issue Date 11 February 2016 16:

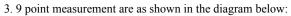
Part Number	Customer	

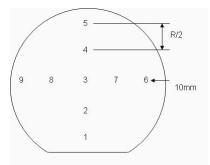
Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.50 mm	
	2.0	Primary Flat Orientation	{110}+/-1 degree	Wafer Vendor
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Secondary Flat Orientation	Semi standard	
	5.0	Overall Thickness	519.00 +/- 11.00 μm	ADE, 100%
	6.0	Total Thickness Variation (TTV)	<5.00μm	Guaranteed by Process
	7.0	Bow	<60.00μm	ADE to ASTM F534, 20%
	8.0	Warp	<60.00μm	ADE to ASTM F657, 20%
	9.0	Edge Chips	0	Bright Light, 100% (note 2)
	10.0	Edge Exclusion	5mm	
HandleSilicon	11.0	Handle Growth Method	CZ	Wafer Vendor
	12.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	13.0	Handle Thickness	500.00 +/- 10.00 μm	ADE, 100%
	14.0	Handle Doping Type	Any	Wafer Vendor
	15.0	Handle Dopant	Any	Wafer Vendor
	16.0	Handle Resistivity	0.005 - 100 Ohmem	Wafer Vendor
	17.0	Backside Finish	Polished with lasermarking	Guaranteed by Process
DeviceSilicon	18.0	Device Growth Method	CZ	Wafer Vendor
	19.0	Device Orientation	{111} +/- 1 degree	Wafer Vendor
	20.0	Nominal Thickness	19.00 +/- 1.00 μm	ADE Single point, 100%
	21.0	Distance to device silicon edge from wafer edge	<= 2.0mm	Typical by Process
	22.0	Device Doping Type	Any	Wafer Vendor
	23.0	Device Dopant	Any	Wafer Vendor
	24.0	Device Resistivity	0.005 - 100 Ohmem	Wafer Vendor
	25.0	Voids	none	Wafer Vendor
	26.0	Scratches	0	Bright Light, 100% (note 2)
	27.0	Haze	none	Bright Light, 100% (note 2)

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Part Number		Customer		
Category	Parameter	Specification	Measurement Method	
Shipping Details	Wafer per box :	Max 25		
	Packaging:	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging		
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness		
Explanatory Notes	1. Microscope inspec	etion performed using microscope scan as below. 5x objective.		
	2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall			

Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.





Additional Information