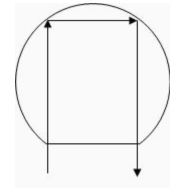
Part Number	Customer

Category		Parameter	Specification	Measurement Method
OverallWafer	1.0	Diameter	100.00 +/- 0.30 mm	
	3.0	Primary Flat Length	32.50 +/- 2.50 mm	Wafer Vendor
	4.0	Primary Flat Orientation	<110> +/- 1deg	Wafer Vendor
	5.0	Secondary Flat Orientation	90deg to primary flat, clockwise when looking at polished device side	wafer vendor
	6.0	Secondary Flat Length	18.0 +/- 2.0 mm	wafer vendor
	7.0	Overall Thickness	310.00 +/- 15.00 µm	ADE, 100%
	8.0	Total Thickness Variation (TTV)	<5.00µm	Guaranteed by Process
	9.0	Bow	<40.00µm	ADE to ASTM F534, 20%
	10.0	Warp	<40.00µm	ADE to ASTM F657, 20%
	11.0	Edge Chips	0	Bright Light, 100% (note 2)
	12.0	Edge Exclusion	5mm	
HandleSilicon	13.0	Handle Growth Method	CZ	Wafer Vendor
	14.0	Handle Orientation	{100} +/- 1 degree	Wafer Vendor
	15.0	Handle Thickness	250.00 +/- 10.00 µm	ADE, 100%
	16.0	Handle Doping Type	P	Wafer Vendor
	17.0	Handle Dopant	Boron	Wafer Vendor
	18.0	Handle Resistivity	>10 Ohmcm	Wafer Vendor
	19.0	Handle TTV	<5.00um	Guaranteed by Process
	20.0	Backside Finish	Polished with NO lasermark	Wafer Vendor
BuriedOxide	21.0	Oxide Type	None	
DeviceSilicon	22.0	Device Growth Method	CZ	Wafer Vendor
	23.0	Device Orientation	{100} +/- 0.5 degree	Wafer Vendor
	24.0	Nominal Thickness	60.00 +/- 2.50 µm	ADE Single Point, 100%
	25.0	Distance to device silicon edge from wafer edge	<= 2.0mm	Typical by Process
	26.0	Device Doping Type	P	Wafer Vendor
	27.0	Device Dopant	Boron	Wafer Vendor
	28.0	Device Resistivity	<0.0015 Ohmcm	Wafer Vendor
	29.0	Resisitivity variation (within wafer)	<8%	Wafer vendor
	30.0	Voids	0	Bright Light, 100% (note 2)
	31.0	Scratches	none	Bright Light, 100% (note 2)
	32.0	Haze	none	Bright Light, 100% (note 2)

Part Number	Customer		
Category	**Parameter**	**Specification**	**Measurement Method**
Shipping Details	Wafer per box :	Max 25	
	Packaging :	Taped Polypropylene Wafer Box Empak, Ultrapak, 100.00mm Antistatic Double Bagging	
	Lot Shipment Data	Device Thickness Bow / Warp Data Handle and SOI Thickness	

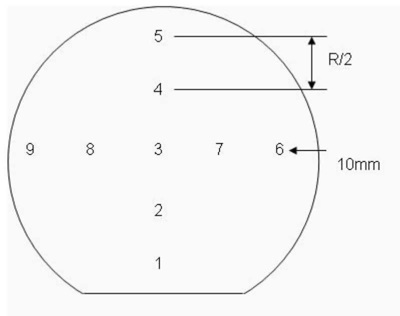
Explanatory Notes

1. Microscope inspection performed using microscope scan as below. 5x objective.



2. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in Overall Wafer, Edge Exclusion. High intensity bright lamp inspection as per ASTM F523.

3. 9 point measurement are as shown in the diagram below:



Additional Information