

### ICE65N950I N-Channel Enhancement Mode MOSFET

RoHS compliant  
2011/65/EU

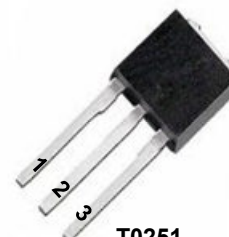
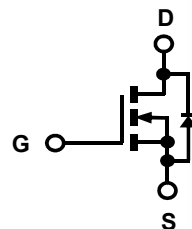


HALOGEN  
FREE

Product Summary			
$I_D$	$T_c=25^\circ\text{C}$	5A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	650V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.75 $\Omega$	Typ
$Q_g$	$V_{DS}=480\text{V}$	22nC	Typ

#### Features

- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High  $dv/dt$  capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



T0251

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

#### Maximum ratings<sup>a</sup> at $T_j=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>b</sup>	$I_D$	$T_c=25^\circ\text{C}$ $T_c=100^\circ\text{C}$	6 3.5	A
Pulsed drain current <sup>c</sup>	$I_{D, pulse}$	$T_c=25^\circ\text{C}$	15	A
Avalanche energy, single pulse	$E_{AS}$	$I_D=2.5\text{A}$	80	mJ
Avalanche current, repetitive	$I_{AR}$	limited by $T_{jmax}$	2	A
MOSFET $dv/dt$ ruggedness	$dv/dt$	$V_{DS}=480\text{V}$ , $I_D=5\text{A}$ , $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	$V_{GS}$	Static	$\pm 20$	V
		AC ( $f>1\text{Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_c=25^\circ\text{C}$	65	W
Operating and storage temperature	$T_j, T_{stg}$		-55 to +150	$^\circ\text{C}$

a Preliminary Data Sheet – Specifications subject to change

b Limited by  $T_{jmax}$  and maximum duty Cycle  $D=0.75$

c Pulse width  $t_p$  limited by  $T_{jmax}$

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

**Thermal characteristics**

Thermal resistance, junction-case	$R_{thJC}$		-	-	1.9	°C/W
Thermal resistance, junction-ambient	$R_{thJA}$	leaded	-	-	68	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

**Electrical characteristics**<sup>a</sup> at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	650	690	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3.1	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$	-	0.04	1	$\mu\text{A}$
		$V_{DS}=650\text{V}, V_{GS}=0\text{V}, T_j=150^\circ\text{C}$	-	14	-	
Gate source leakage current	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$r_{DS(on)}$	$V_{GS}=10\text{V}, I_D=2.5\text{A}, T_j=25^\circ\text{C}$	-	0.75	0.95	$\Omega$
		$V_{GS}=10\text{V}, I_D=2.5\text{A}, T_j=150^\circ\text{C}$	-	2.2	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	3.8	-	$\Omega$

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	625	-	pF
Output capacitance	$C_{oss}$		-	59	-	
Reverse transfer capacitance	$C_{rss}$		-	1.2	-	
Transconductance	$g_{fs}$	$V_{DS}>2 \cdot I_D \cdot R_{DS}, I_D=2.5\text{A}$	-	4	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=480\text{V}, V_{GS}=10\text{V}, I_D=5\text{A}, R_G=4\Omega \text{ (External)}$	-	22	-	ns
Rise time	$t_r$		-	23	-	
Turn-off delay time	$t_{d(off)}$		-	52	-	
Fall time	$t_f$		-	18	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

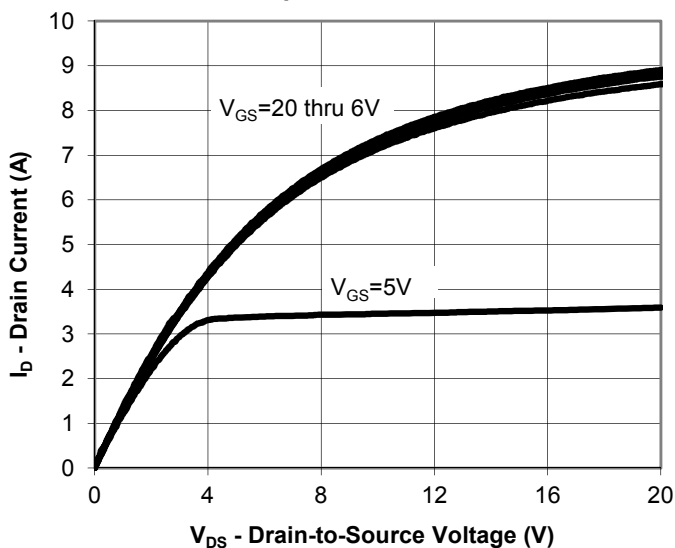
### Gate charge characteristics

Gate to source charge	$Q_{gs}$	$V_{DS}=480\text{ V}, I_D=5\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	3.6	-	nC
Gate to drain charge	$Q_{gd}$		-	7.9	-	
Gate charge total	$Q_g$		-	22	-	
Gate plateau voltage	$V_{plateau}$		-	5.1	-	V

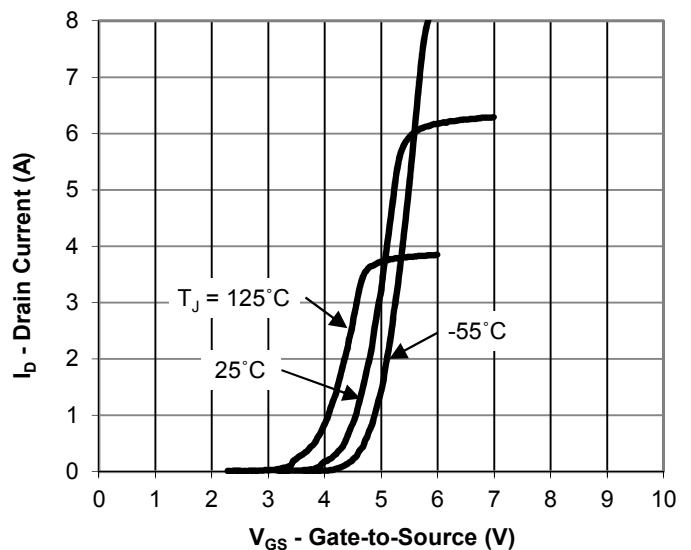
### Reverse Diode

Continuous forward current	$I_S$	$V_{GS}=0\text{ V}$	-	-	5	A
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_S=I_F$	-	0.8	1.2	V
Reverse recovery time	$t_{rr}$	$V_{RR}=100\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{ S}$	-	240	-	ns
Reverse recovery charge	$Q_{rr}$		-	2.5	-	$\mu\text{ C}$
Peak reverse recovery current	$I_{rm}$		-	20	-	A

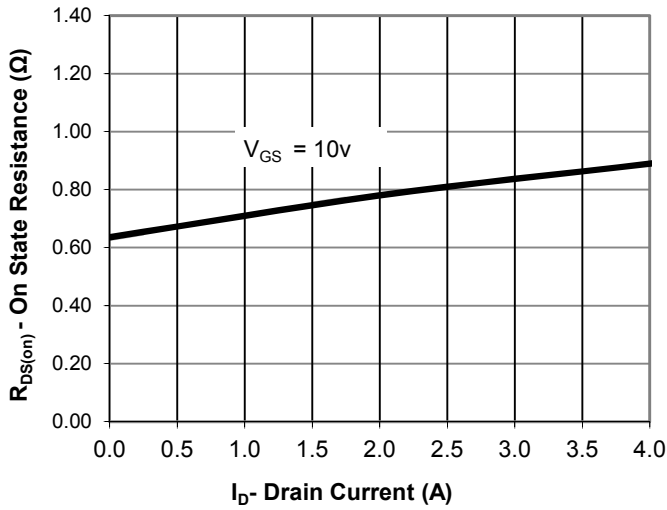
**Output Characteristics**



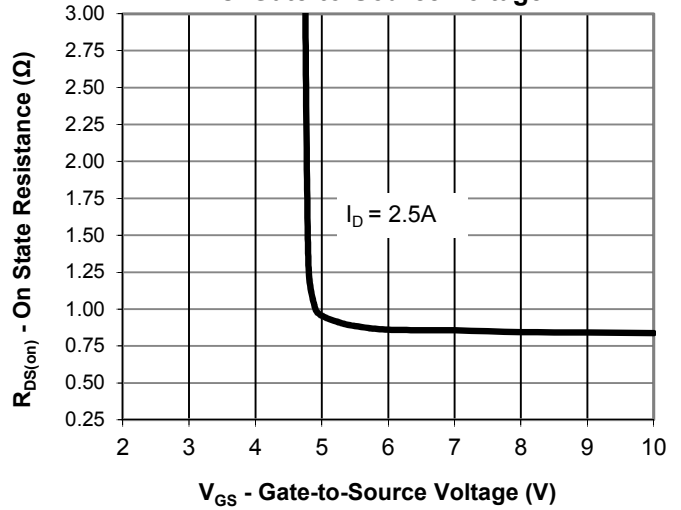
**Transfer Characteristics**



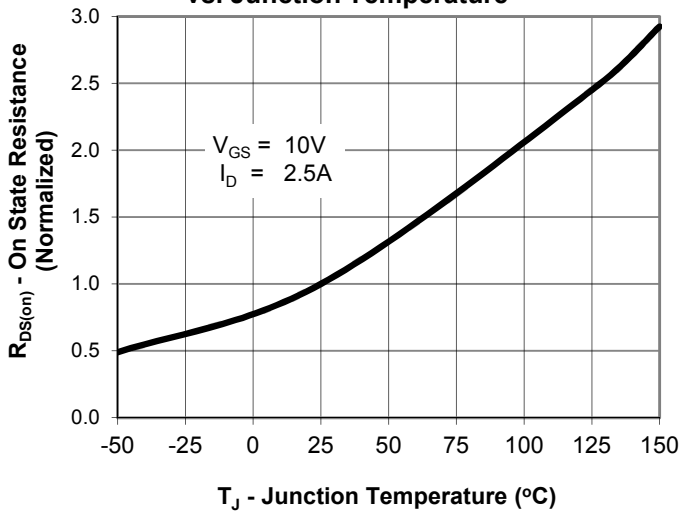
**Drain-Source On-State Resistance vs. Drain Current**



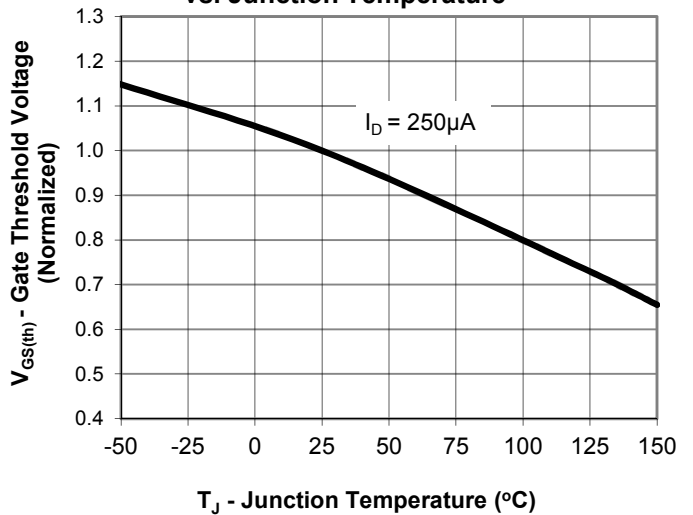
**Drain-Source On-State Resistance vs. Gate-to-Source Voltage**



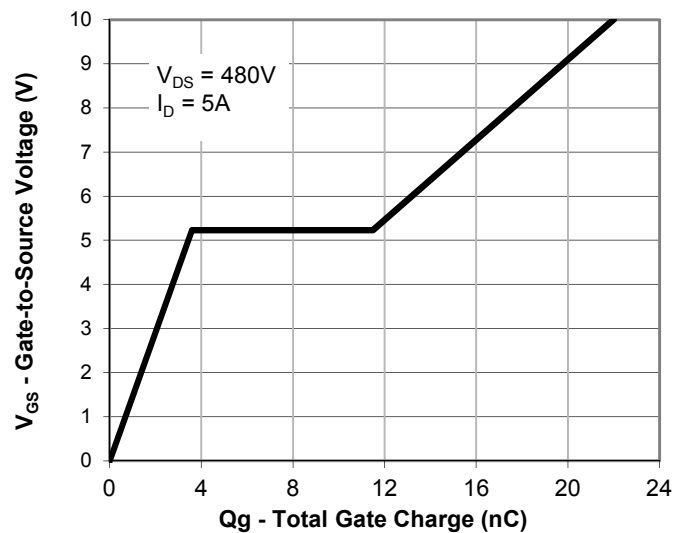
**Drain-Source On State Resistance vs. Junction Temperature**



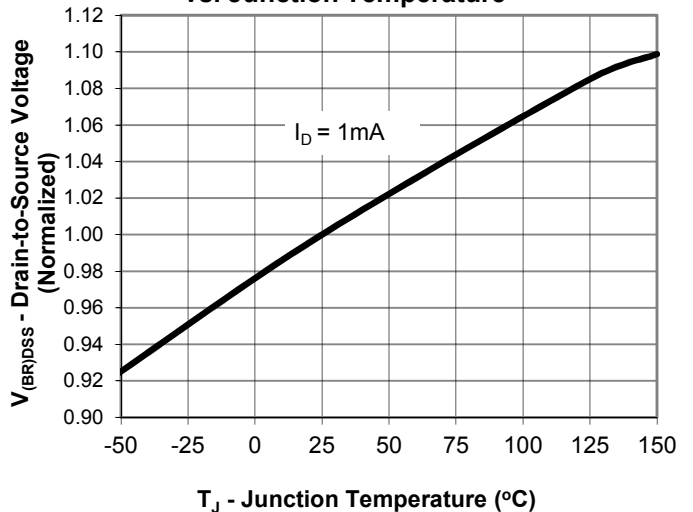
**Gate Threshold Voltage vs. Junction Temperature**



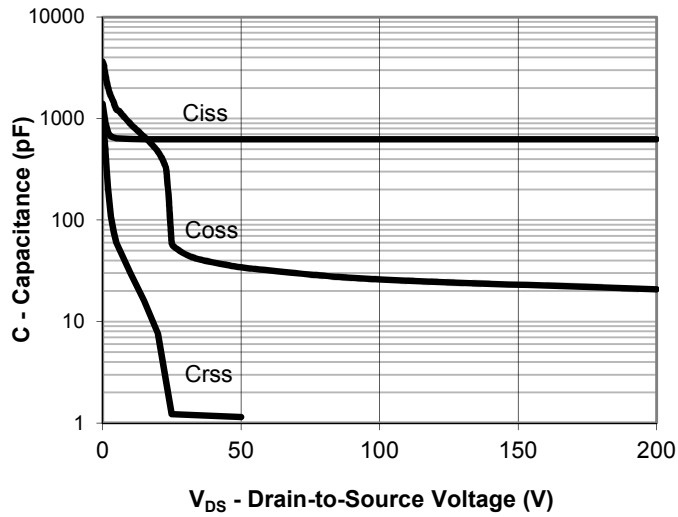
**Gate Charge**



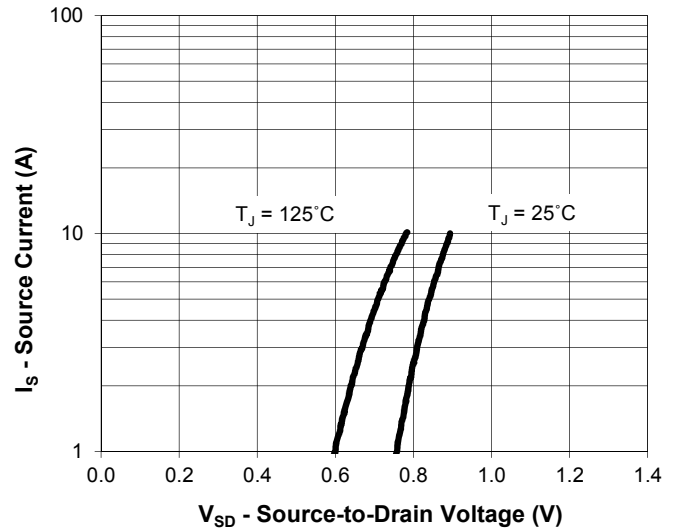
**Drain-to-Source Breakdown Voltage vs. Junction Temperature**



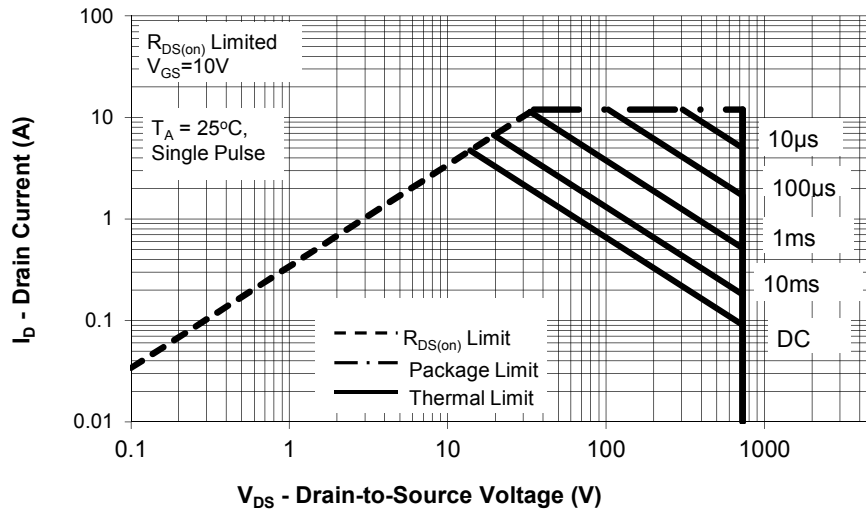
**Capacitance**



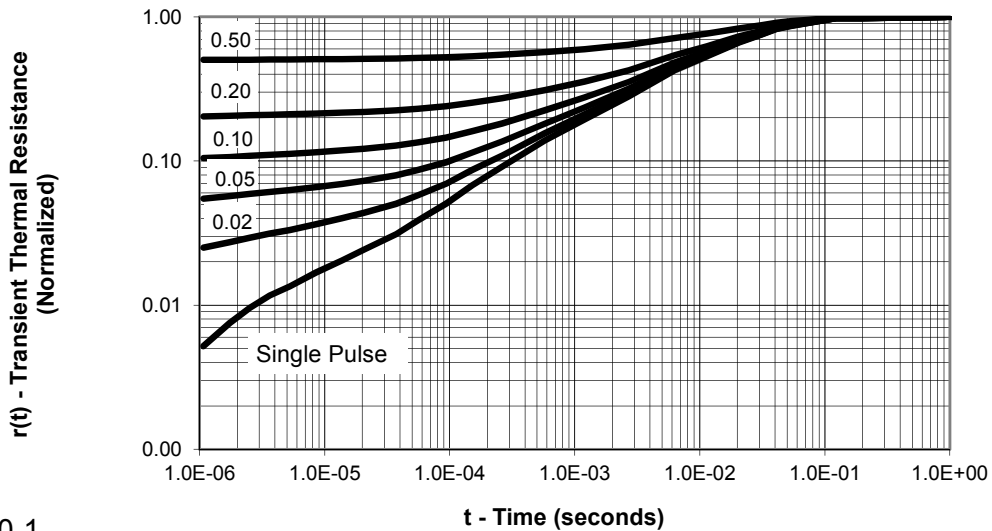
**Source-Drain Diode Forward Voltage**

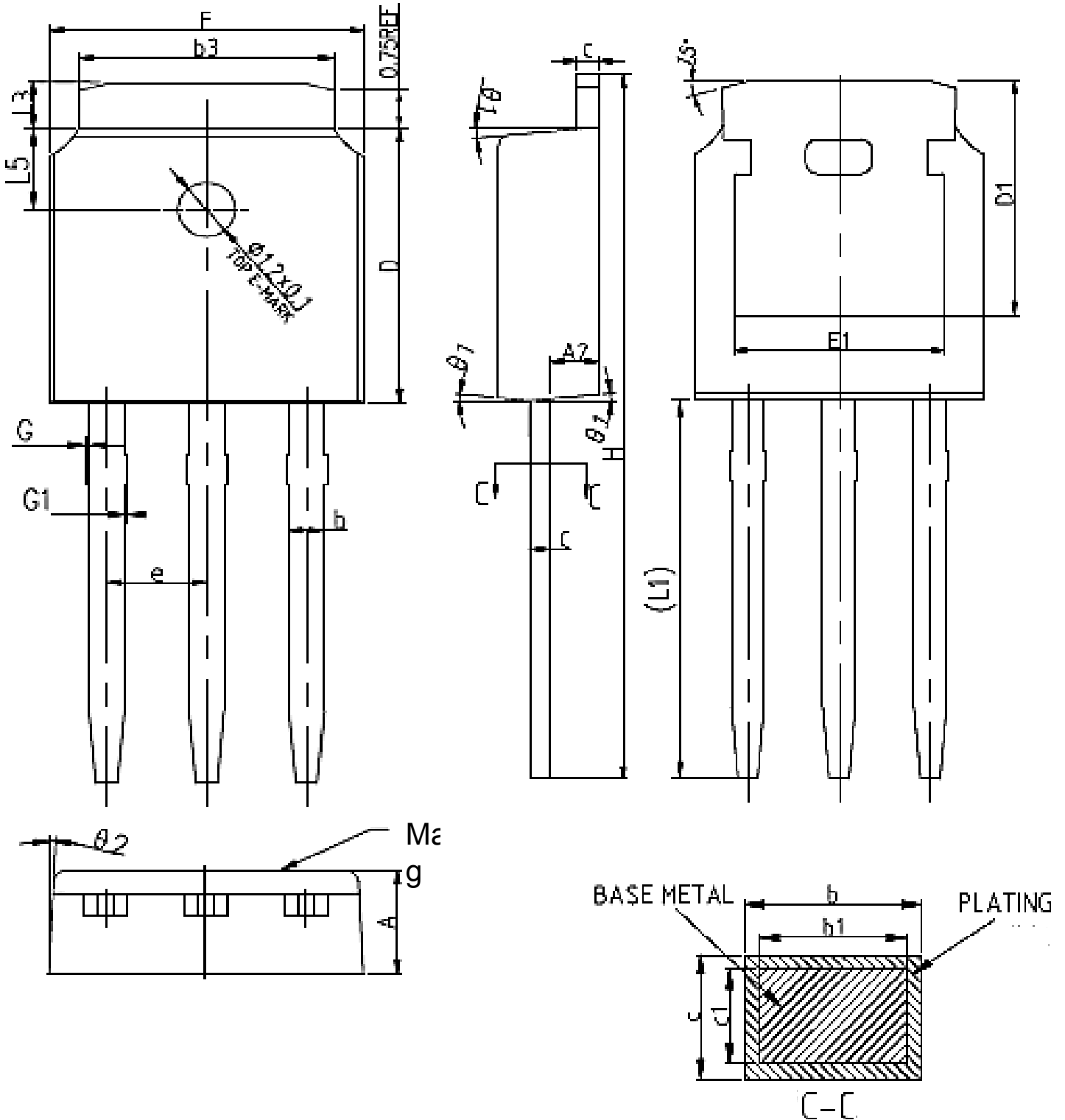


**Maximum Rated Forward Biased Safe Operating Area**



**Transient Thermal Response, Junction-to-Ambient**





## COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
<b>A</b>	<b>2.20</b>	<b>2.30</b>	<b>2.38</b>
<b>A2</b>	<b>0.97</b>	<b>1.07</b>	<b>1.17</b>
<b>b</b>	<b>0.72</b>	<b>0.78</b>	<b>0.85</b>
<b>b1</b>	<b>0.71</b>	<b>0.76</b>	<b>0.81</b>
<b>b3</b>	<b>5.23</b>	<b>5.33</b>	<b>5.46</b>
<b>c</b>	<b>0.47</b>	<b>0.53</b>	<b>0.58</b>
<b>c1</b>	<b>0.46</b>	<b>0.51</b>	<b>0.56</b>
<b>D</b>	<b>6.00</b>	<b>6.10</b>	<b>6.20</b>
<b>D1</b>	<b>5.30 REF</b>		
<b>E</b>	<b>6.50</b>	<b>6.60</b>	<b>6.70</b>
<b>E1</b>	<b>4.70</b>	<b>4.83</b>	<b>4.92</b>
<b>e</b>	<b>2.286 BSC</b>		
<b>H</b>	<b>16.10</b>	<b>16.40</b>	<b>16.60</b>
<b>L1</b>	<b>9.20</b>	<b>9.40</b>	<b>9.60</b>
<b>L3</b>	<b>0.90</b>	<b>1.02</b>	<b>1.25</b>
<b>L5</b>	<b>1.70</b>	<b>1.80</b>	<b>1.90</b>
<b>θ1</b>	<b>5°</b>	<b>7°</b>	<b>9°</b>
<b>θ2</b>	<b>5°</b>	<b>7°</b>	<b>9°</b>

## ICEMOS SUPERJUNCTION PATENT PORTFOLIO

### ICEMOS GRANTED PATENTS

US7,429,772  
US7,439,178  
US7,446,018  
US7,579,607  
US7,723,172  
US7,795,045  
US7,846,821  
US7,944,018  
US8,012,806  
US8,030,133

### 3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2  
US7,023,069B2  
US7,364,994  
US7,227,197B2  
US7,304,944B2  
US7,052,982B2  
US7,339,252  
US7,410,891  
US7,439,583  
US7,227,197B2  
US6,635,906  
US6,936,867  
US7,015,104  
US9,109,110  
US7,271,067  
US7,354,818  
US7,052,982,  
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.



## Marking Information

**YY** = Last two digits of the year

**WW** = Work week calendar on Icemos subcon assembly & test house

**\*** = Initial for Icemos subcon assembly and test house

**XXXXXX** = Lot ID

**ICE65N950** = ICE is Icemos logo and 65N950 is a designated device part number

