IceMOS Trench SOI

Cooler than Cool

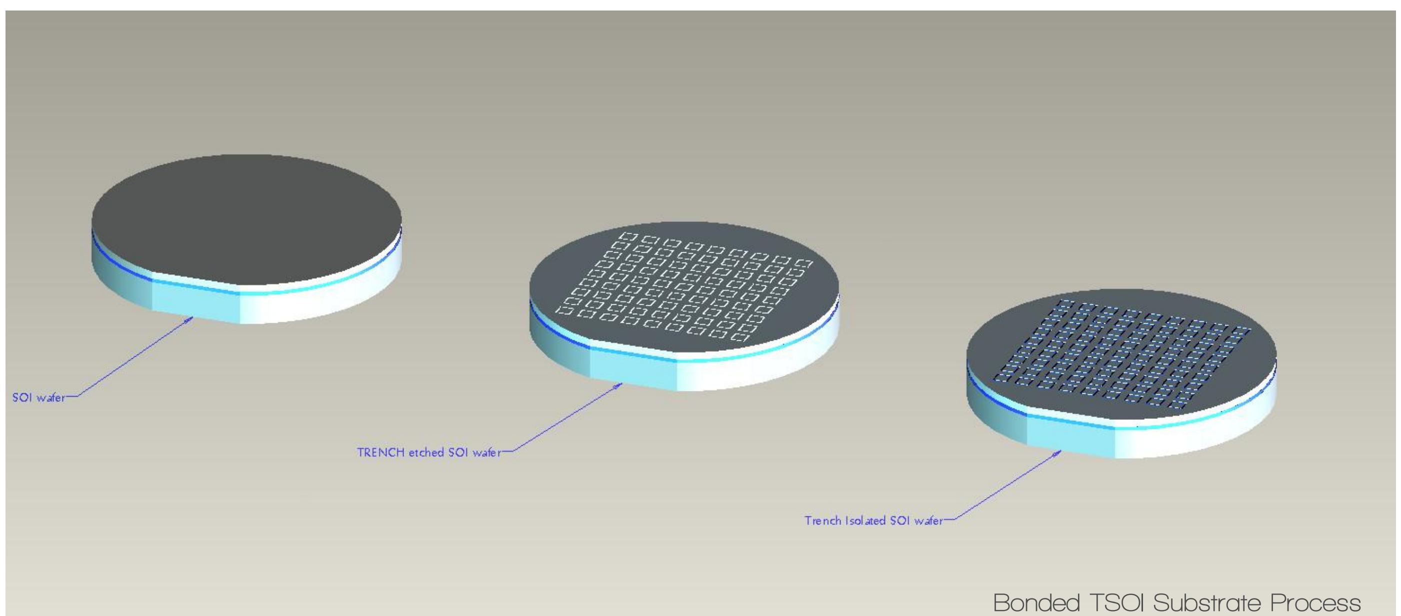
IceMOS Technology presents its dielectric isolation technology – delivering high voltage isolation between components on the same chip. Isolation is achieved using thick film SOI technology combined with state of the art high aspect ratio deep trench etching and oxide/poly refill. This technology is available on all wafer sizes from 100mm to 150mm and silicon device layers from 1.5um to 100um.

Applications

- MEMS devices
- Solid State Relay photovoltaic generators
- Photovoltaic cells and Optoelectronic devices/ICs
- High Voltage analog ICs for telecommunications
- High performance bipolar circuits
- Smart Power ICs
- Integrated Sensors

Key Features

- Complete device isolation
- Allows significant die shrink compared with conventional Junction isolation
- Much lower defect density than conventional DI technologies
- Lower Substrate capacitance than bulk
- Lower cost than trench isolation on epi



Bonded TSOI Substrate Process

5 Hannahstown Hill, Belfast, BT17 0LT, United Kingdom Phone +44 2890 574773 www.icemostech.com

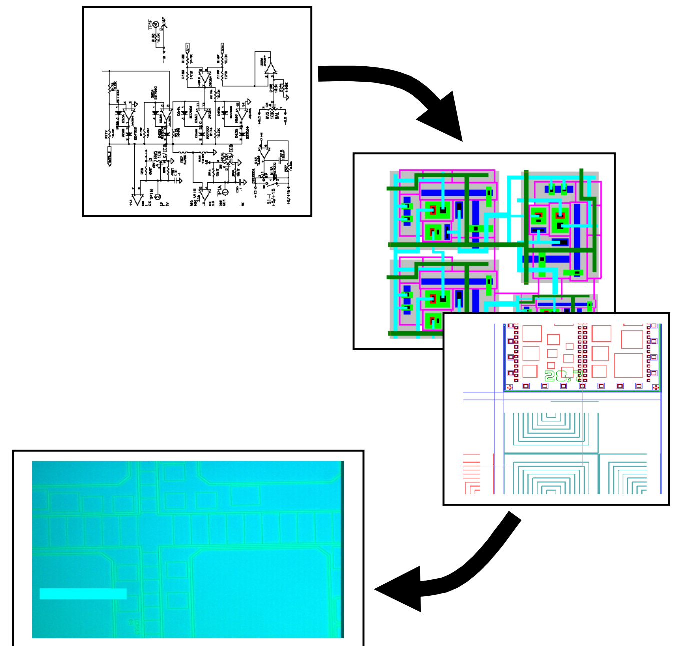
5 Hannahstown Hill, Belfast, BT17 0LT, United Kingdom Phone +44 2890 574773 www.icemostech.com

Supply Options Available

- Provision of DI Substrate from isolation mask provided
- Provision of Fully processed DI IC using ICEMOS as foundry to complete post isolation processing
- Provision of Full IC design and fabrication on DI from customer schematic

Post Isolation technologies available

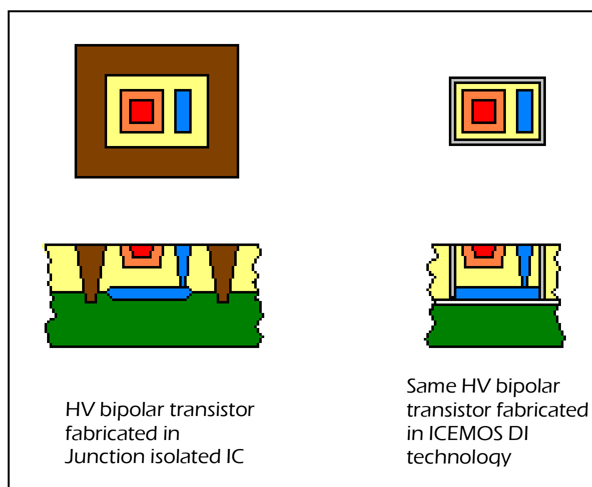
- Simple Bipolar
- CMOS (1P, 2M)
- BiCMOS (1P, 2M)



The IceMOS trench-isolated silicon-on–insulator (SOI) substrate provides complete dielectric isolation of tubs. Key benefits are:

- Elimination of buried layer.
- Elimination of epi layer.
- Elimination of P+ isolation diffusion.
- Minimizing of parasitic capacitances.
- High quality crystalline silicon layer.
- Simultaneous increase of die per wafer.
- High voltage breakdown capability.
- Customised trench patterns.

Our process engineers will work closely with your design group to realize the full potential for your processes.



Comparison of HV bipolar IC transistors made on junction isolated and ICEMOS DI technologies, showing 3x saving in silicon real estate

Dielectric Isolation IC Specification

Parameter	Specification Range
Wafer diameter	100, 125, 150
Handle Thickness	350 – 1000 µm
Handle Thickness Tolerance	+/- 5 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Stack Thickness	≤1200 µm
Resistivity	<0.001 – >10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Backside finish	Lapped/etched or Polished
Thermally Oxidised Buried Oxide Thickness	0.2 – 5.0 µm grown on Handle, Device or both wafers
Device Layer Thickness	1.5 – 100 µm
Tolerance	+/- 0.5 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	<0.001 – >10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Buried Layer Implant	N-Type or P-Type up to $1e^{16}cm^{-2}$
Trench Mask tone	Positive resist
Trench Mask type	E-beam master for projection aligner
Trench line width	>2um
Trench Aspect ratio	15:1
Trench Sidewall doping type	Phosphorus & Boron
Trench refill – oxide (each sidewall)	0.1 – 1.0 µm
Trench refill – polysilicon	To fill (Doped or undoped Polysilicon)
Planarisation	CMP
Final field oxide	Thermal oxide + TEOS up to 2.0 µm

The above is a standard IceMOS specification; however, we are always happy to work with our customers to engineer specific solutions. If you would like to discuss an alternative specification, please contact our sales team: sales@icemostech.com