Engineered Silicon Substrates Selector Guide

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Contents

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SOI Solutions

Applications

Our customised SOI solutions are used in the following fields:

- Advanced pressure sensors
- Accelerometers
- Gyroscopes
- Microfluidics/flow sensors
- RF MEMS
- MOEMs/Optical MEMs
- Optoelectronics
- Smart Power
- Advanced Analog ICs
- Microphones
- Luxury watches

End Markets:

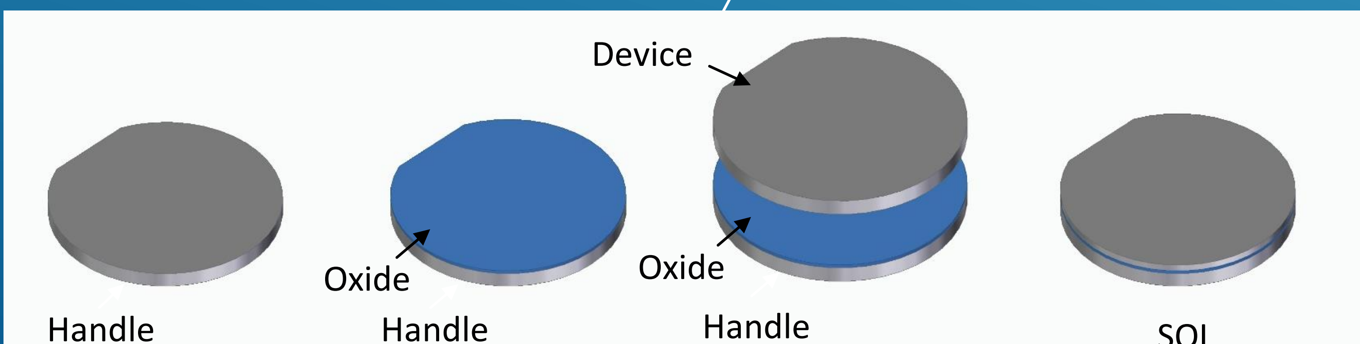
- Telecommunications
- Medical
- Automotive
- Consumer
- Instrumentation

IceMOS Technology is a leading supplier of 100-200mm thick-film Silicon on Insulator wafers for a large range of IC and MEMS applications. With over 20 years' experience in SOI manufacturing, we offer an impressive specification range, which is amongst the widest available in the market.

We have extensive experience in a variety of SOI substrates and our highly skilled applications engineering team is available to assist you to select the optimum combination of parameters for your requirements, ensuring that you receive the perfect custom SOI solution for your application.

By making continuous improvements to our processes in a Lean Six Sigma environment, IceMOS Technology offer world class product quality, competitive cost structure plus rapid turnaround makes IceMOS Technology your ideal SOI partner.

SOI Wafer with <1.5mm edge terrace



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SOI Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150 mm	200 mm
Handle Layer Specifications		
Handle Thickness	200–1100 µm	450-1100 µm
Handle Thickness Tolerance	±5 µm	
Stack Thickness	280–1150 µm	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Backside Finish	Lapped/Etched or Polished	
Buried Oxide Specifications		
Thermally Oxidised Buried Oxide Thickness	0.2 – 4.0 µm grown on Handle, Device or both wafers	
Device Layer Specifications		
Device Layer Thickness	≥1.5 µm	≥5 µm
Tolerance	± 0.5 µm	±0.8 µm
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Buried Layer Implant	N type or P type	

The above is a standard IceMOS specification; however, we are always happy to work with our customers to engineer specific solutions. If you would like to discuss an alternative specification, please contact our sales team: sales@icemostech.com

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SiSi Solutions

Applications

- High Voltage PIN Diodes
- RF Attenuators
- Photo Detectors
- X-Ray Detectors
- IR Sensors
- HV Power Devices
- Replacement for Epitaxial layers

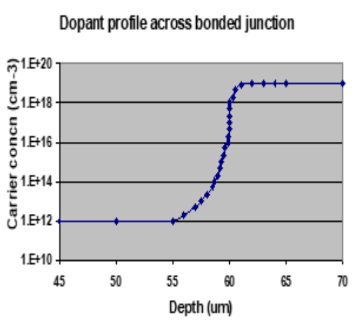
Key Features:

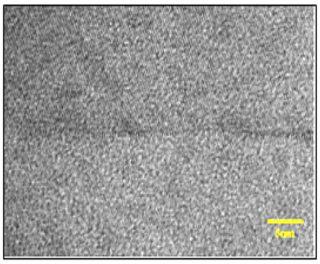
- High Quality
- Low cost
- Low defect density
- Excellent Layer uniformity
- Multiple layers
- Sharp transitions
- Layer resistivity up to 10kΩ-cm
- Excellent interface quality – verified by high resolution SAM Inspection

For semiconductor device manufacturers, the IceMOS Silicon – Silicon Direct bonded wafer offers a cost effective alternative to thick epitaxial layers and inverse epi that have traditionally been used for applications such as power devices and PiN diodes.

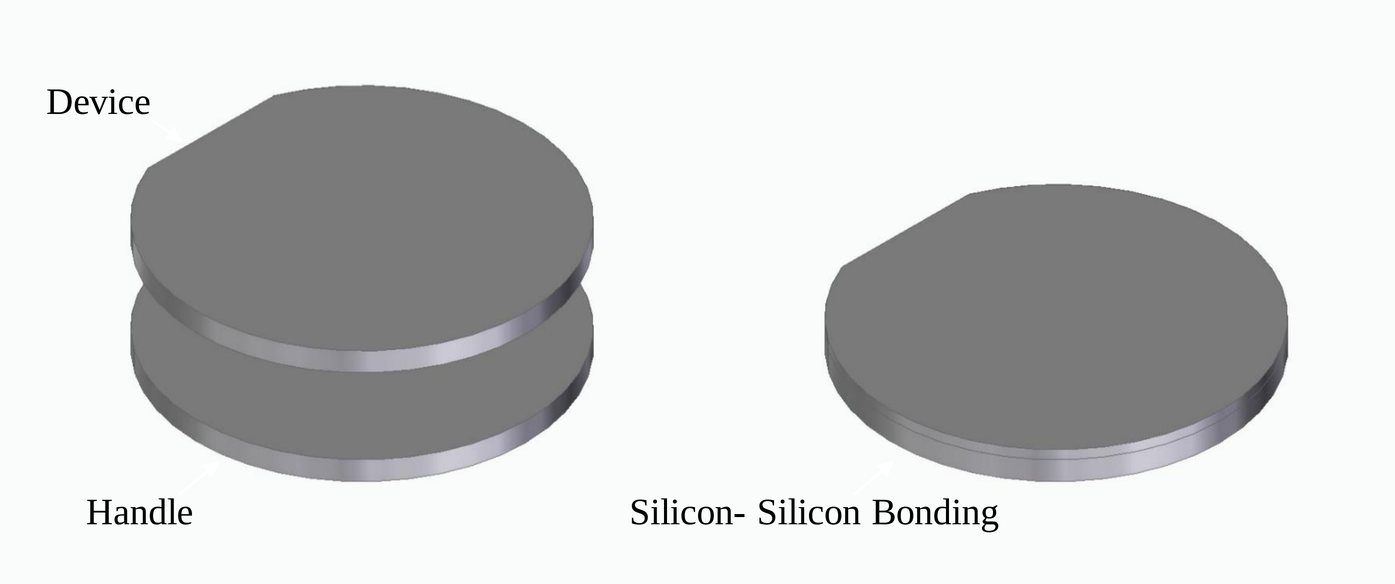
The use of direct wafer bonding technology allows silicon substrates to be produced containing multiple layers of single crystal silicon. These layers can have a resistivity range 1mΩ-cm to 10kΩ-cm, N and P-type and can include combinations of orientations – a feature not possible with conventional epitaxial wafers.

The IceMOS SiSi bonding process gives a high quality wafer with low leakage, low warp and a low defect density. Additionally, the thickness variation in the layers can be as little as +/-0.5um. The transition between high and low dopant levels can be sharp or soft, depending on the application or customer requirement.





High resolution TEM image of SiSi wafer interface



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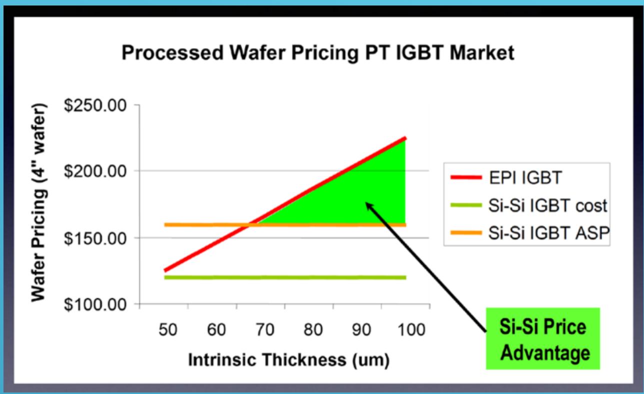

This chart shows the cost advantage of SiSi direct wafer bonding over Epi layers as a starting material for many electronic devices. This makes SiSi wafers an advantageous option for performance and cost reduction.

SiSi Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150 mm	200 mm
Handle Layer Specifications		
Handle Thickness	200–1100 µm	450-1100 µm
Handle Thickness Tolerance	±5 µm	
Stack Thickness	280–1150 µm	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Backside Finish	Lapped/Etched or Polished	
Device Layer Specifications		
Device Layer Thickness	≥20 µm	≥20 µm
Tolerance	± 0.5 µm	±0.8 µm
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Buried Layer Implant	N type or P type	

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DSOI Solutions

Applications

Our customised Double SOI (DSOI) solutions are used in the following fields:

- SOI solutions for MEMS/MST
- Microfluidics/flow sensors
- RF MEMS
- MOEMs
- Optoelectronics
- Optical MEMS

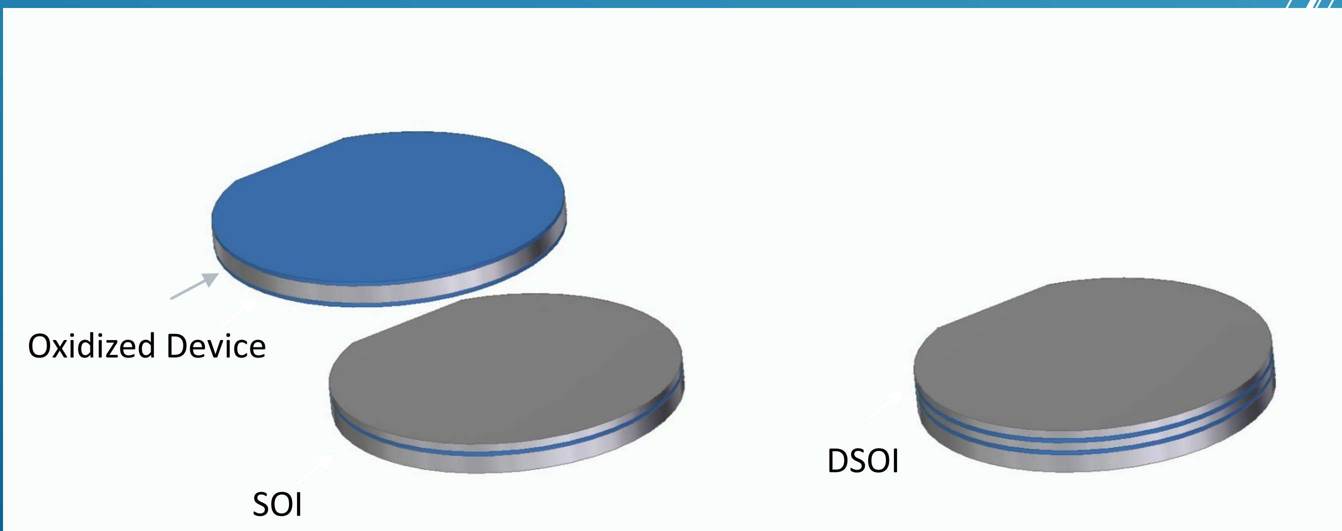
End Markets:

- Telecommunications
- Medical
- Automotive
- Consumer
- Security

IceMOS Technology is a leading supplier of Double or Multi-Layer SOI for a large range of IC and MEMS applications. With over 20 years' experience in SOI manufacturing, we offer an impressive specification range, which is amongst the widest available in the market, ensuring that you receive the perfect DSOI solution for your application. We have extensive experience in SOI substrates, and our applications engineering expertise can help you select the best combination of parameters to aid your downstream processing of the DSOI engineered substrate.

With a flexible approach, IceMOS allows the customer to grow from R&D production (offering small lots) to volume production. Our experienced MEMS process engineers have experience in optical, inertial, and other MEMS fields. IceMOS Technology offer additional foundry processing for MEMS, trench isolation, buried cavity, layer release, etc.

By making continuous improvements to our processes in a Lean Six Sigma environment, IceMOS Technology offer world class product quality, competitive cost structure plus rapid turnaround makes IceMOS Technology your ideal DSOI partner.



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DSOI Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150 mm	200 mm
Handle Layer Specifications		
Handle Thickness	200–1100 µm	450-1100 µm
Handle Thickness Tolerance	±5 µm	
Stack Thickness	280–1150 µm	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Backside Finish	Lapped/Etched or Polished	
Buried Oxide Specifications		
Thermally Oxidised Buried Oxide Thickness	0.2 – 4.0 µm grown on Handle, Device or both wafers	
Device Layer Specifications (1st and 2nd Layer)		
Device Layer Thickness	≥1.5 µm	≥5 µm
Tolerance	± 0.5 µm and ± 1 µm	±0.8 µm and ± 1.6 µm
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Buried Layer Implant	N type or P type	

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DSP Solutions

IceMOS uses over 20 years of experience to offer the marketplace world class custom DSP solutions (Double Sided Polished).

Our highly skilled team has many years of design and manufacturing experience to help develop a DSP solution to your requirement.

IceMOS DSP wafers are an excellent substrate for double sided lithography processing; the IceMOS expertise and knowledge of the product and the processes allow for exceptional thickness control and surface roughness – ideal for a downstream wafer bonding process. Additionally, non-standard specifications for demanding applications will always be considered.

Our world class product quality, competitive cost structure plus rapid turnaround makes IceMOS Technology your ideal DSP partner.

Applications

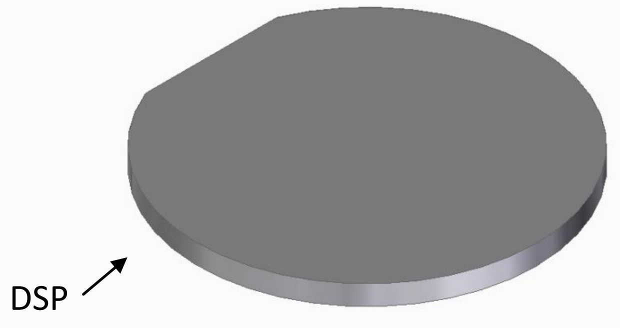
Our customised Double-Sided Polished substrates are used in the following fields:

-

- DSP solutions for MEMS/MST
- Microfluidics/flow sensors
- RF MEMS
- Optoelectronics

End Markets:

- Telecommunications
- Medical
- Automotive
- Consumer
- Security



Wafer can be oxidised if required

DSP Specification

Parameter	Specification Range	
Wafer Diameter	100, 125, 150mm	200mm
Wafer Thickness	300–1150 µm	450-1150 µm
Wafer Thickness Tolerance	±2 µm	±5 µm
Total Thickness Variation (TTV)	≤1 µm	≤2 µm
Bow	≤40 µm	
Warp	≤40 µm	
Roughness	≤2Å	
Dopant Type	N or P	
Doping	N type: Phos, Red Phos, Sb & As P type: Boron	
Resistivity	≤0.001 – ≥10000 Ω-cm	
Growth Method	CZ, MCZ or FZ	
Crystal Orientation	<100>, <111> or <110>	
Thermally Oxidised Field Oxide Thickness	0.2-4.0 µm	

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CSOI Solutions

Applications

Our customised SOI solutions are used in the following fields:

-

- Advanced pressure sensors
- Inertial MEMS
- Microfluidics
- Resonators
- Microphones

End Markets:

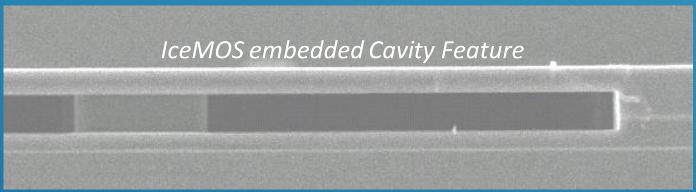
- Telecommunications
- Medical
- Automotive
- Consumer
- Instrumentation

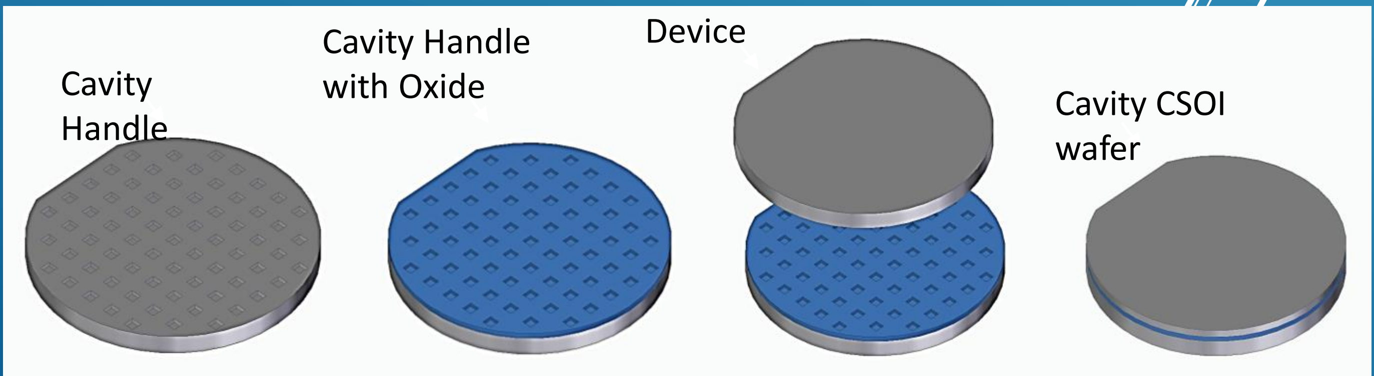
IceMOS Technology is a leading supplier of 100–150mm Cavity Bonded SOI wafers for a large range of MEMS applications. By utilising years of deep silicon trench etch expertise and experience coupled with our advanced wafer bonding technology allow customer cavity expectations to be materialized into innovative products.
The IceMOS Cavity Bonded SOI is a pre-etched feature embedded under a silicon membrane. This provides an opportunity for the customer designers to develop more intelligent devices to meet the most demanding markets.

Our Cavity Bonded SOI solutions allow the customer to take advantage of –

- IceMOS' superior bonding technology and expertise.
- Reduce any stiction issues at release.
- Simplified manufacturing flows.
- Low Cost Cavity SOI/Si-Si Solutions.
- Flexibility in construction around customer needs/ downstream applications.

IceMOS can offer various methods of constructing the Cavity Bonded SOI Solutions to optimize customer cavity requirements. C-SAM and AVI inspection can be included as desired.
We also have the added advantage of incorporating advanced features into Cavity Bonded SOI solutions which potentially opens possibilities that might otherwise not have been considered.





C-SAM and AVI inspection available

CSOI Specification

Parameter	Specification Range
Wafer Diameter	100, 125, 150 mm
Handle Layer Specifications	
Handle Thickness	200–1100 µm
Handle Thickness Tolerance	±5 µm
Stack Thickness	280–1150 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Backside Finish	Lapped/Etched or Polished
Buried Oxide Specifications	
Thermally Oxidised Buried Oxide Thickness	0.2 – 4.0 µm grown on Handle, Device or both wafers
Device Layer Specifications	
Device Layer Thickness	≥1.5 µm
Tolerance	± 0.5 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Buried Layer Implant	N type or P type
Membrane Thickness/SOI Thickness	>2 µm
Membrane Tolerance	+/-0.5 µm
Cavity Span: Membrane Thickness	<50:1 µm (dependent on design)
Minimum Bonding Size Features	20 µm
Alignment Accuracy of Cavity to Alignment Marks	+/-3 µm
Cavity Depth	1-30 µm @ +/-10% 31-300 µm @ +/-20%
Cavity Location	Handle, Device or Buried Oxide

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Thin-SOI Solutions

Applications

Our customised Thin-SOI solutions are suitable for the following fields:

- RF Filters
- Optoelectronics
- Image Sensing
- Wireless Connectivity
- Flexible-Hybrid Electronics
- RF MEMS

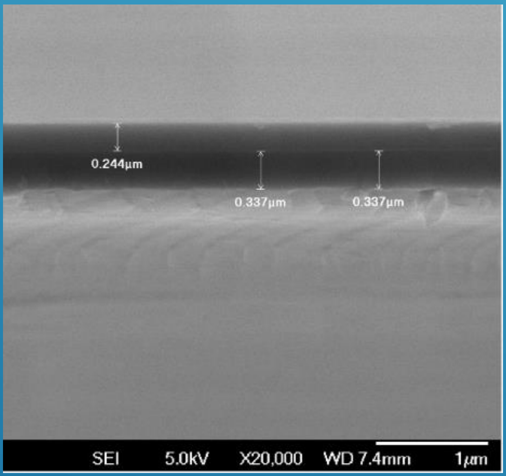
End Markets:

- Telecommunications
- Consumer
- Power
- Medical

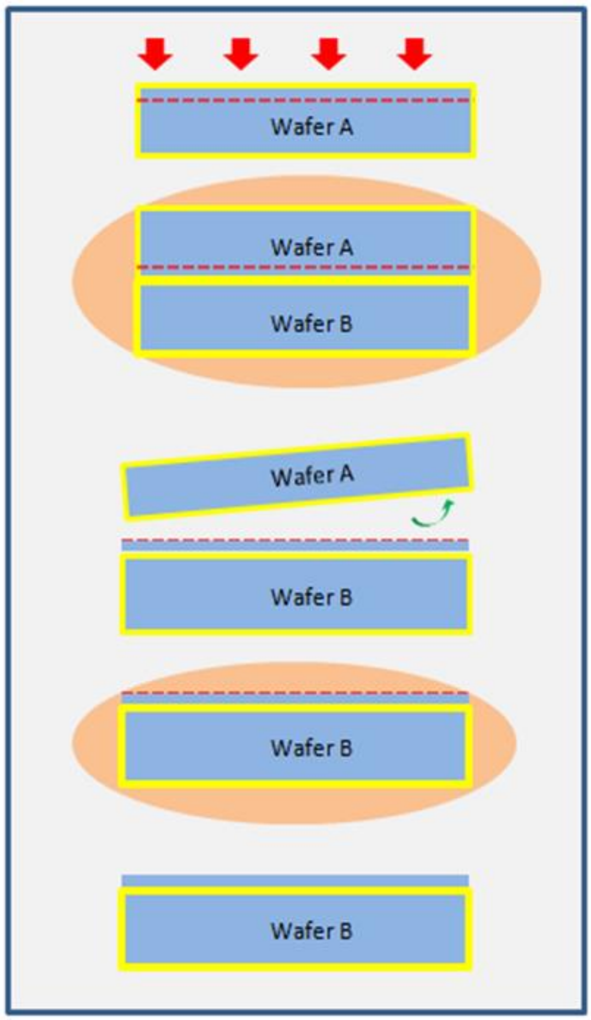
IceMOS Technology has developed and is offering a Thin-SOI wafer range with device layers < 1µm. Building on the 20+ years of SOI manufacturing experience, IceMOS is offering the same high-quality product as our existing Thick-SOI wafers for RF Applications.

With the wide range of specifications for both silicon wafers and the thermally grown Buried Oxide Layer, the IceMOS Thin-SOI wafer range covers applications such as Silicon Photonics to SAW filters.

By making continuous improvements to our processes in a Lean Six Sigma environment, IceMOS Technology offer world class product quality, competitive cost structure plus rapid turnaround makes IceMOS Technology your ideal SOI partner.



SEM image of IceMOS 245nm Thin-SOI Wafer



1. Implantation
2. Bonding
3. Cleaving
4. Heat Treatment
5. CMP

Thin-SOI Specification

Parameter	Specification Range
Wafer Diameter	150 - 200 mm
Handle Layer Specifications	
Dopant Type	N or P
Doping	N type: Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Buried Oxide Specifications	
Thermally Oxidised Buried Oxide Thickness	0.1um – 2µm grown on Device or both wafers
Buried Oxide Uniformity	± 5%
Device Layer Specifications	
Device Layer Thickness	0.1um – 1um
Device Layer Uniformity	± 20nm
Dopant Type	N or P
Doping	N type: Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>

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Trench SOI

Applications

- MEMS devices
- Solid State Relay photovoltaic generators
- Photovoltaic cells and Optoelectronic devices/ICs
- High Voltage Analog ICs for telecommunications
- High performance bipolar circuits
- Smart Power ICs
- Integrated Sensors

Key Features:

- Complete device isolation
- Allows significant die shrinkage compared with conventional Junction isolation
- Much lower defect density than conventional DI technologies
- Lower Substrate capacitance than bulk
- Lower cost than trench isolation on epi

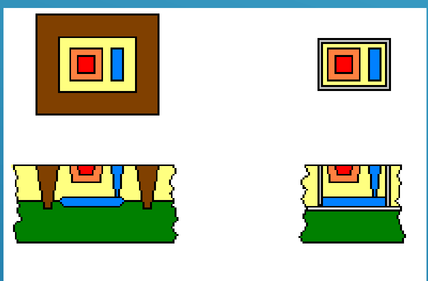


Illustration shows a comparison of HV bipolar IC transistors made on junction isolated and ICEMOS DI technologies, showing 3x saving in silicon real estate.

HV bipolar transistor fabricated in Junction isolated IC

Same HV bipolar transistor fabricated in ICEMOS DI technology

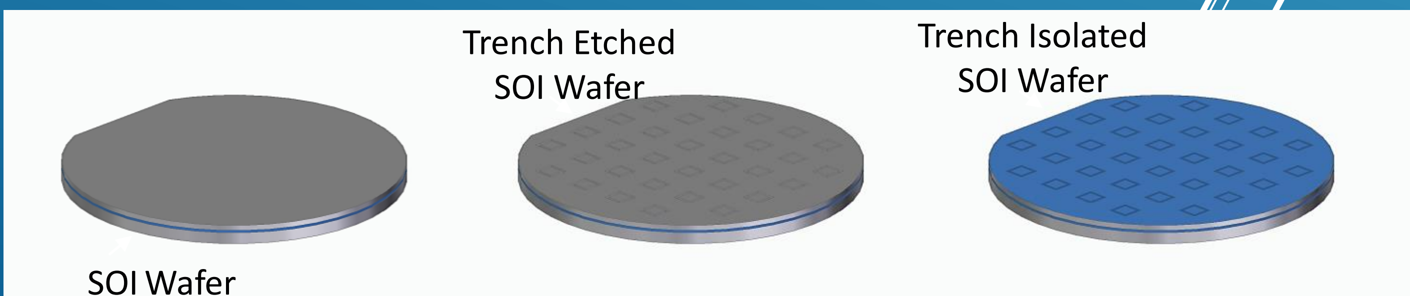
IceMOS Technology presents its dielectric isolation technology – delivering high voltage isolation between components on the same chip. Isolation is achieved using thick film SOI technology combined with state-of-the-art high aspect ratio deep trench etching and oxide/poly refill. This technology is available on all wafer sizes from 100mm to 150mm and silicon device layers from 1.5um to 100um.

<u>Supply Options Available</u>
Provision of DI Substrate from isolation mask provided
Provision of Fully processed DI IC using ICEMOS as foundry to complete post isolation processing
Provision of Full IC design and fabrication on DI from customer schematic

<u>Post Isolation technologies available</u>
- Simple Bipolar
- CMOS (1P, 2M)
- BiCMOS (1P, 2M)

The IceMOS trench-isolated silicon-on-insulator (SOI) substrate provides complete dielectric isolation of tubs.
Key benefits are:
- Elimination of buried layer
- Elimination of epi layer
- Elimination of P+ isolation diffusion
- Minimizing of parasitic capacitances
- High quality crystalline silicon layer
- Simultaneous increase of die per wafer
- High voltage breakdown capability
- Customised trench patterns

Our process engineers will work closely with your design group to realize the full potential for your processes.



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Trench SOI Specification

Parameter	Specification Range
Wafer Diameter	100, 125, 150 mm
Handle Layer Specifications	
Handle Thickness	350–800 µm
Handle Thickness Tolerance	±5 µm
Stack Thickness	350–1150 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Backside Finish	Lapped/Etched or Polished
Buried Oxide Specifications	
Thermally Oxidised Buried Oxide Thickness	0.2 – 4.0 µm grown on Handle, Device or both wafers
Device Layer Specifications	
Device Layer Thickness	1.5 - 100 µm
Tolerance	± 0.5 µm
Dopant Type	N or P
Doping	N type: Phos, Red Phos, Sb & As P type: Boron
Resistivity	≤0.001 – ≥10000 Ω-cm
Growth Method	CZ, MCZ or FZ
Crystal Orientation	<100>, <111> or <110>
Buried Layer Implant	N type or P type
Trench Mask Tone	Positive Resist
Trench Mask Type	E-beam master for projection aligner
Trench Line Width	> 2um
Trench Aspect Ratio	15:1
Trench Sidewall Doping Type	Phosphorus
Trench Refill – Oxide (each sidewall)	0.1 – 1.0 µm
Trench Refill – Polysilicon	To Fill (Doped or undoped Polysilicon)
Planarisation	CMP
Final Field Oxide	Thermal oxide + TEOS up to 1um

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TSV Solutions

Applications

Our customised Through Silicon Via solutions are used in the following fields:

- SOI solutions for MEMS/MST
- Microfluidics/flow sensors
- RF MEMS
- Optoelectronics
- Smart Power
- Advanced Analog ICs

End Markets:

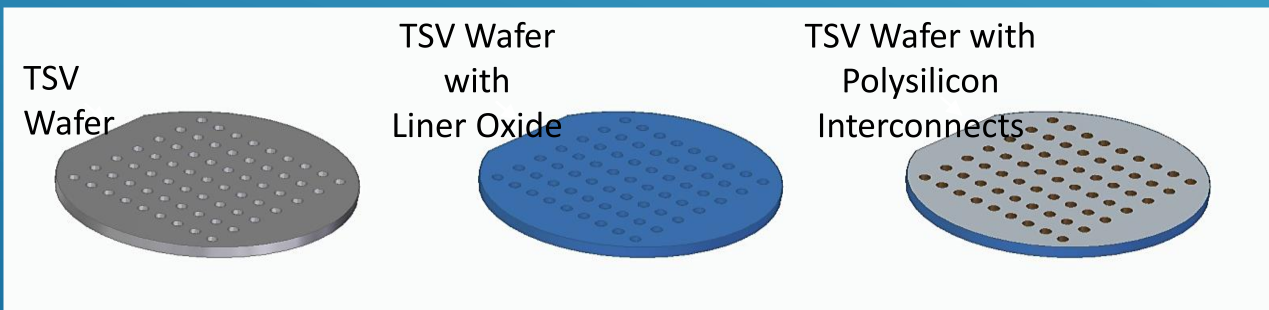
- Telecommunications
- Medical
- Automotive
- Consumer
- Instrumentation

IceMOS Technology have developed an innovative and powerful through-wafer interconnect technology which can allow device designers in both standard IC and MEMS device industries overcome packaging problems associated with their designs. Using this interconnect solution allows many of our customers to migrate their designs easily to a wafer level package with solder bumped contacts.

The IceMOS Technology solution is a pre-processed substrate which is delivered to the customer with the interconnect already formed within the substrate. This substrate is fully CMOS compatible.

All interconnect is performed using through wafer etching and refill and heavily doped polysilicon. The wafers meet all standard specifications for surface metallic contamination, planarity and particle count. We have verified stable substrate performance up to diffusion temperatures of 1200C.

IceMOS will develop customer specific through-wafer interconnect solution in partner, taking the preferred interconnect pattern and implementing it on the wafer for easy connectivity to a circuit or sensor. The TSV may be beside or below existing bond pads. The design is optimised and fully customised to the customer's requirements.



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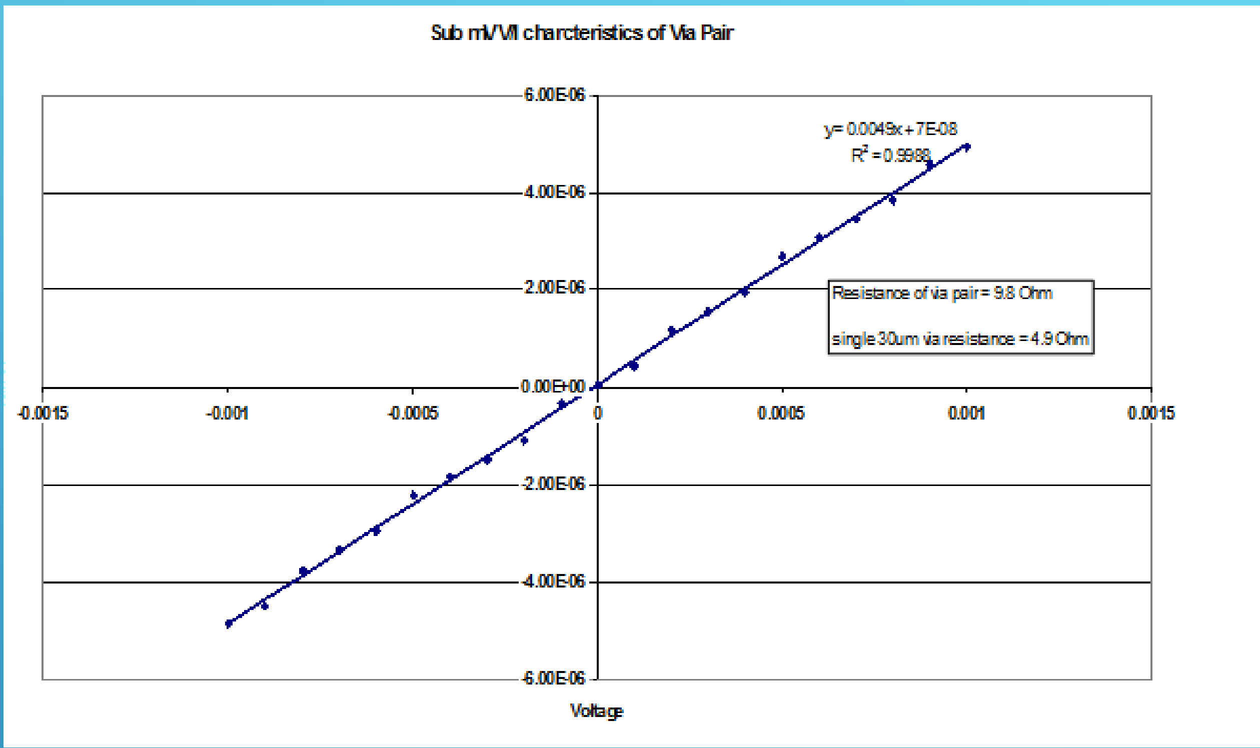

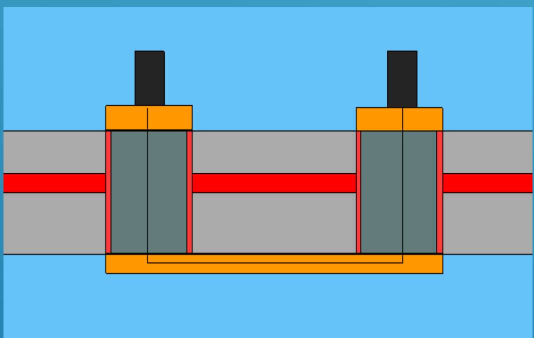

Vias directly connected top and bottom using Al-Si metallisation – no additional implants/diffusions. Characteristic shows completely Ohmic behaviour even at very low current levels.

TSV Specification

Parameter	Specification Range
Aspect Ratio of Via	<15:1
Wafer Diameter	100mm & 150mm
Wafer Thickness	300-525µm
Max. Diameter	40µm on smallest side
Min. Pitch	90µm (3x via width)
Poly Resistivity	<5 mΩ-cm
Isolation Resistance	Determined by oxide liner (design dependent)
Oxide Liner Thickness	0.2-2µm

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Foundry Services

Key Features:

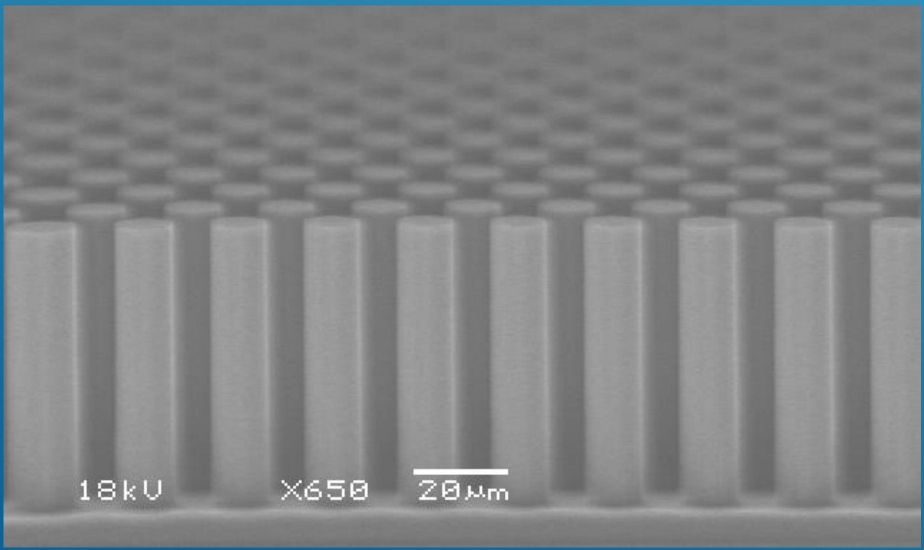
- High Quality
- Low cost
- Low defect density
- Multiple layers
- Process sequences specific to customer requirements can be offered

IceMOS Technology offers a wide range of additional processing services for customers who simply require a high-quality single unit process to be performed on their own wafers.

IceMOS offers high resolution SAM (Scanning Acoustic Microscope) imaging of our bonded BSOI and CSOI wafers, this can also be offered as a service for customer's own bonded wafers. SAM inspection offers a means of non-destructive imaging of the bonded interface. In contrast to common non-destructive test methods such as conventional ultrasonic test methods, infrared microscopy and x-ray microscopy, Scanning Acoustic Microscopes scan the specimen surface pixel to pixel, line to line and detect with a special transducer the reflected ultrasonic waves out of the specimen. IceMOS SAM inspection offers a detection limit in the range of 10µm lateral size of delamination with a delaminated height in the range of 15nm. IceMOS can offer high resolution whole wafer scanning on wafer diameters 100mm – 200mm with a pixel size as small as 20 µm. Individual areas of the wafer can be scanned at higher resolutions.

IceMOS Technology will use engineering expertise to develop a process flow and CAD (Computer Aided Design) layout used to develop a new set of masks or cross-sectional concept drawings.

The standards of IceMOS unit process foundry services are unsurpassed by any other foundry. With processes operated within an IATF 16949 manufacturing environment, controlled to tight tolerances by Statistical Process Control (SPC) and within contamination standards required by advanced CMOS, IceMOS offers you the perfect solution. All this is supported by a fast turnaround service and high compliance on On-Time-Delivery.



Example of IceMOS high density etch pillars.

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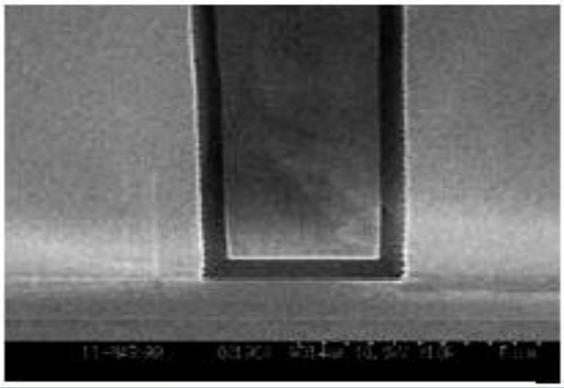
DRIE Etch Services

Deep trench etch is a core technology of IceMOS. With over 20 years' experience in this field, IceMOS Technology can offer DRIE Silicon etch options with minimum feature size 2um, on SOI up to 300um thick, trenches with aspect ratios of 20:1, large area patterns on SOI and Si wafers with exposed areas up to 65% and up to 500um through wafer etching on bulk Si and on SOI with aspect ratios up to 12:1. If required, our refill technology will not only ensure a completely filled trench, but will also leave a fully planar silicon surface for subsequent processing. Examples of just a small sample of what we can do are shown below. Contact our engineering team to discuss etch depth, sidewall angle, aspect ratio, exposed etch area and whether you require refill.

Neighbouring High and Low aspect ratio trenches in SOI without undercut.



Conformal Oxide & Poly refill in trenches etched in SOI.

Thin Film Depositions & Diffusion

Excellent process control and a suite of High temperature thermal oxidation and LPCVD TEOS oxide and LPCVD polysilicon allow IceMOS to offer excellent facilities for those wishing to refill etched features or deposit stacks of thermal or sacrificial oxide layers and heavily n++ doped or undoped LPCVD Polysilicon layers.

Process	Diameter	Min Thickness	Max Thickness	Tolerance (+/-)	Notes
Dry Oxidation	100mm, 125mm, 150mm & 200mm	24nm	200nm	15%	
Wet Oxidation	100mm, 125mm, 150mm & 200mm	100nm	6000nm	5%	
Undoped LPCVD Polysilicon	100mm, 125mm & 150mm	200nm	4500nm	10%	Per deposition
Heavily doped LPCVD Polysilicon (n++)	100mm, 125mm & 150mm	200nm	4500nm	10%	Per deposition
LPCVD TEOS	100mm, 125mm & 150mm	200nm	1000nm	5%	Densification at 1050C optional

The above is a standard IceMOS specification; however, we are always happy to work with our customers to engineer specific solutions. If you would like to discuss an alternative specification, please contact our sales team: sales@icemostech.com

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"Cooler than Cool"TM